

Compal Confidential

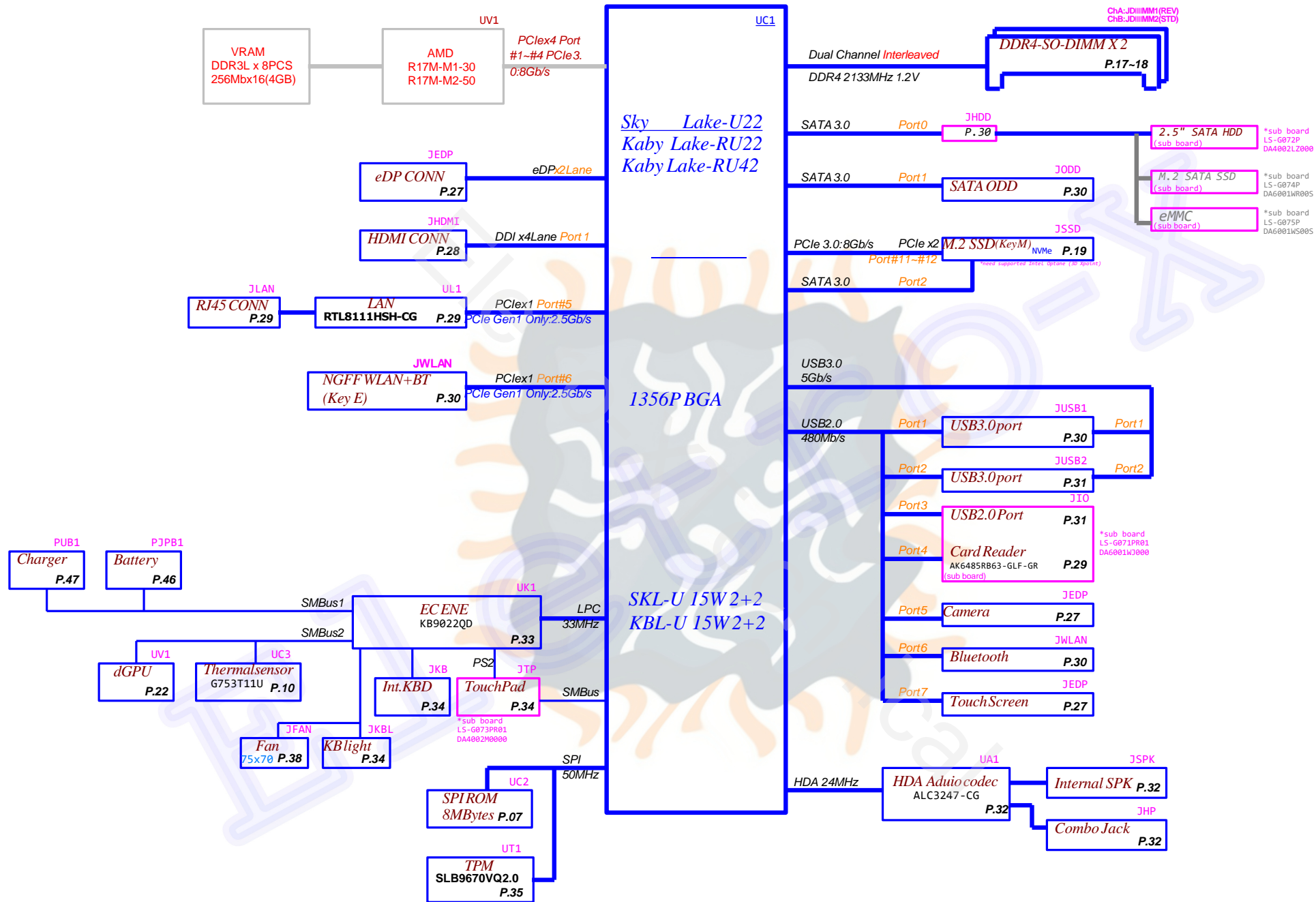
CSL50 Schematics Document

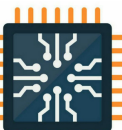
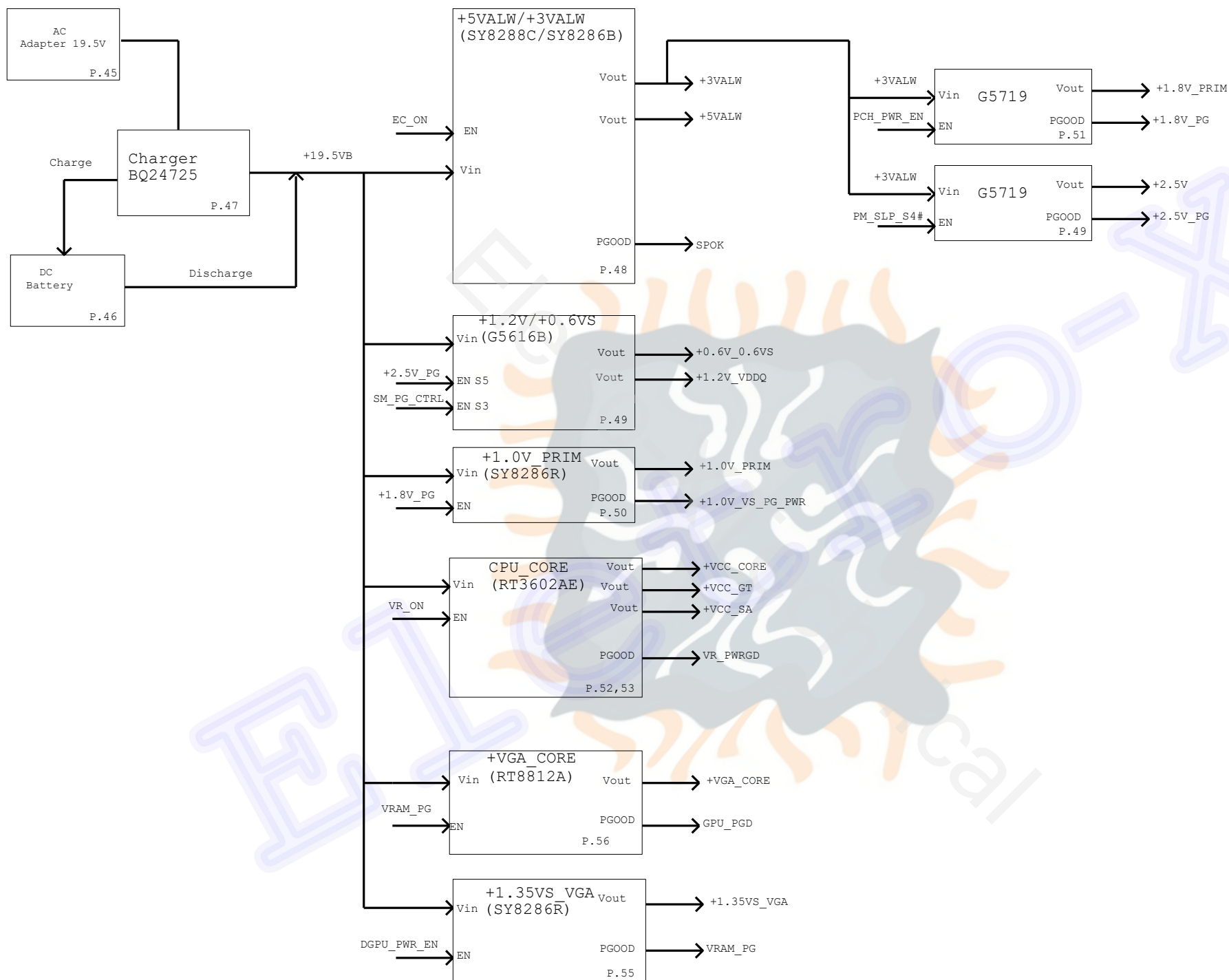
Sky Lake-U(2+2)-DDR4 SODIMMx2
GPU AMD R17M-M1-30
R17M-M2-50
(DDR3L 4GB)

Date : 2018-01-08 REV : 1.0

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Issued Date	2015/10/22	Deciphered Date	2017/10/22	Title	Cover Page
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				Date	Monday, January 08, 2018
				Sheet	1 of 450



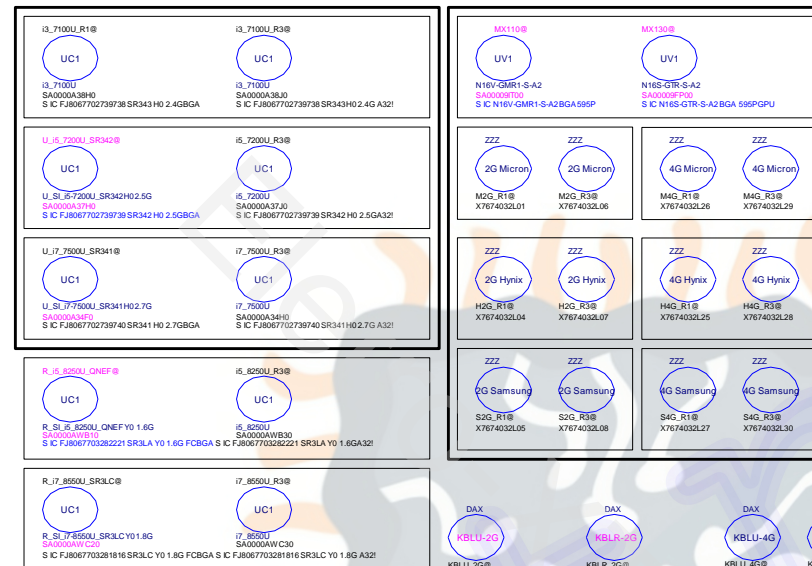




SOC_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
SMBCLK SMBDATA	+3V_PRIM	DIMM1	0x50	0xA0	0xA1
		DIMM2	0x52	0xA4	0xA5
		TouchPAD	0x2C	0x58	0x59

EC_SMBUS Port	Power Rail	Device	Address (7 bit)
SMBUS Port 1	+3VL_EC	BAT	0x16
		CHGR	0x12
SMBUS Port 2	+3VS	dGPU	
		Thermal Sensor	0x90
		PCH	

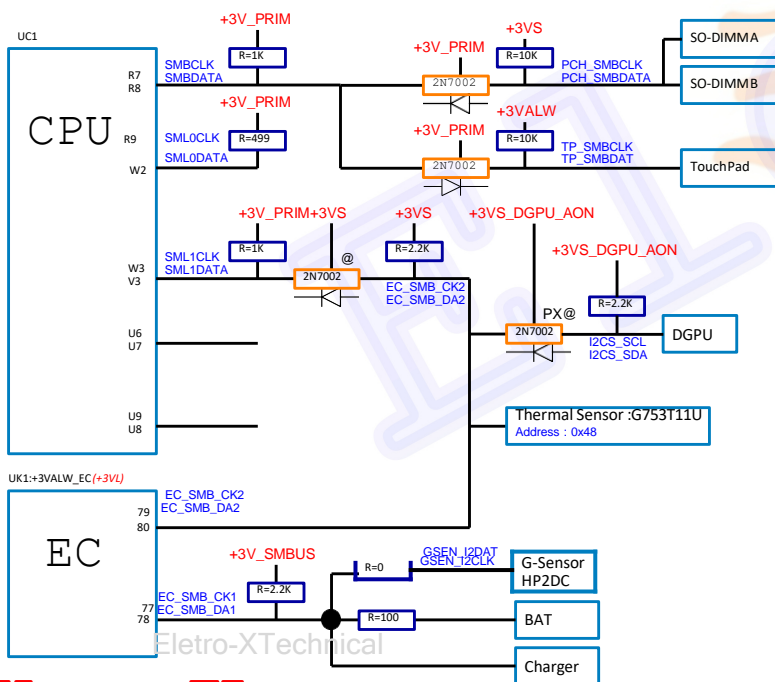
Function	Stuff	Un-Stuff
DGPU SKU	PX@	
UMA SKU	UMA@	
TPM	TPM@	



STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (FullON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SoftOFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB2.0port	DESTINATION
1	USB3.0Type-C
2	USB2.0/USB3.0
3	USB2.0/USB3.0
4	BT
5	HD/IR_1/IR_2Camera
6	IR_2Camera
7	Card Reader
8	X
9	X
10	X

Lane#	PCI-E	SATA	USB3.0	DESTINATION	CLK
1			1	USB3.0Type-C	X
2			2	USB3.0Type-C	X
3			3	USB2.0/USB3.0	X
4			4	USB2.0/USB3.0	X
5	1		5	GPU(DI5only)	CLK0
6	2		6	GPU(DI5only)	
7	3			GPU(DI5only)	
8	4			GPU(DI5only)	
9	5			LAN	CLK1
10	6			WLAN	CLK2
11	7	0		HDD	X
12	8	1a		ODD	CLK3
13	9			X	X
14	10			X	X
15	11	1b		X	CLK4
16	12	2		NVMe x2 SATASSD	X

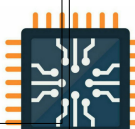
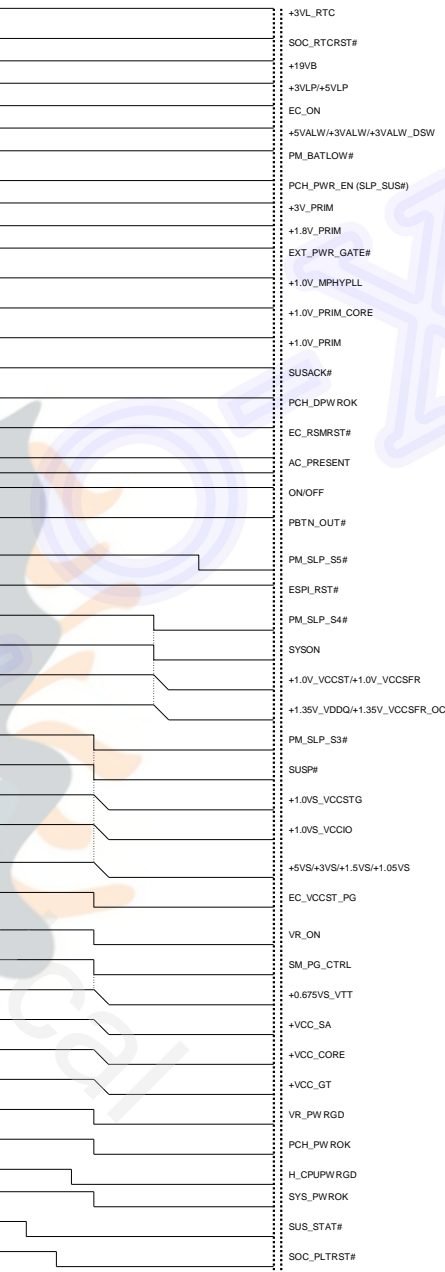
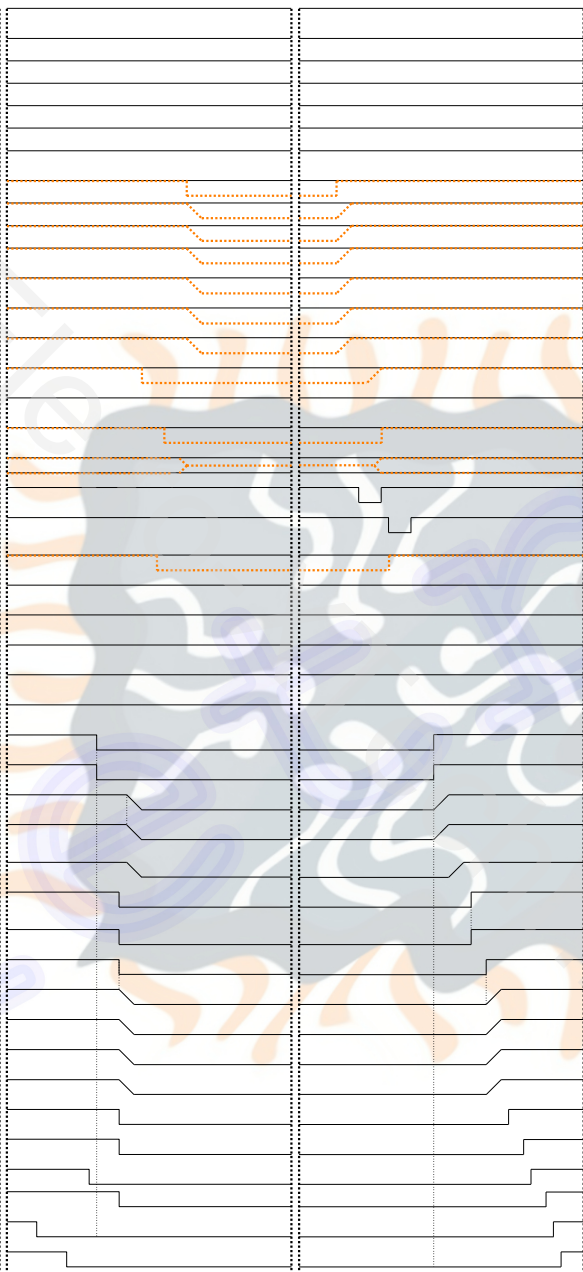
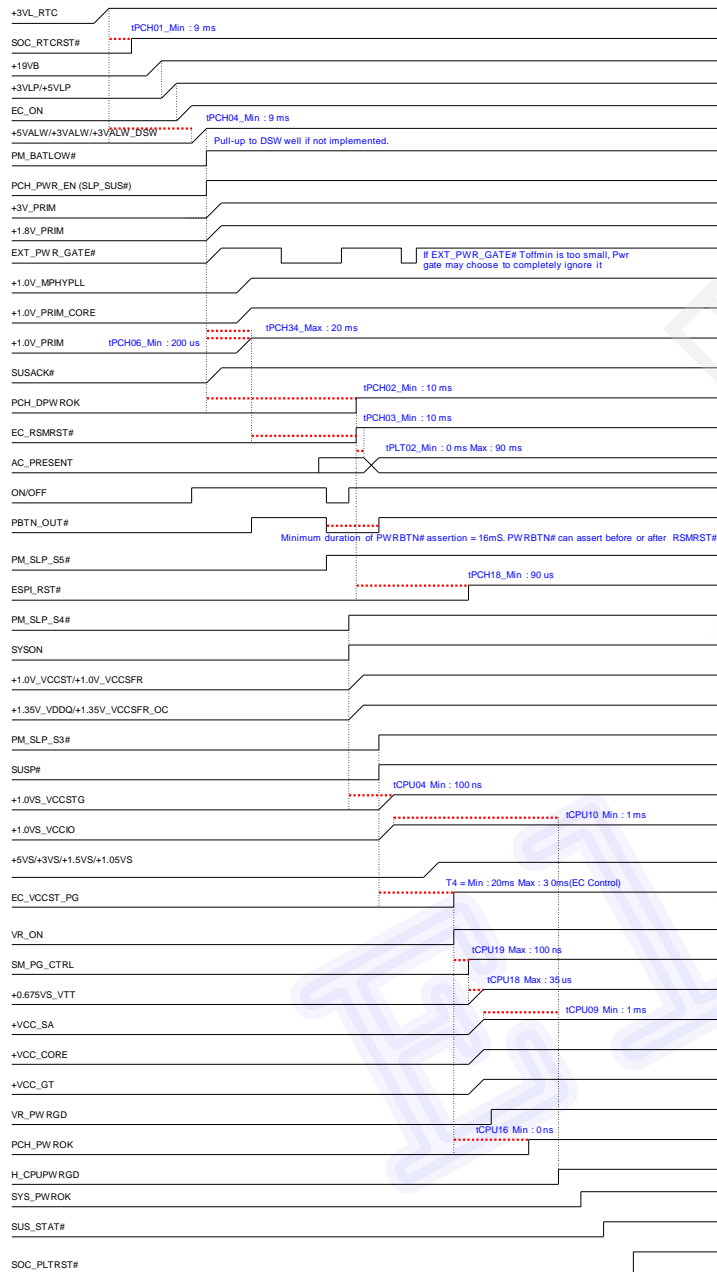


G3->S0

S0->S3/DS3

S0/DS3->S0

S0->S5



SOC_DP1_CTRL_DATA (Internal Pull Down):

Display Port B Detected

0 = Port B is not detected.

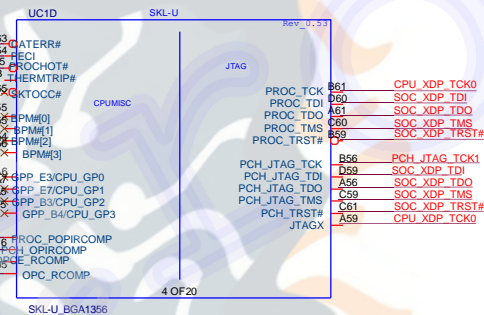
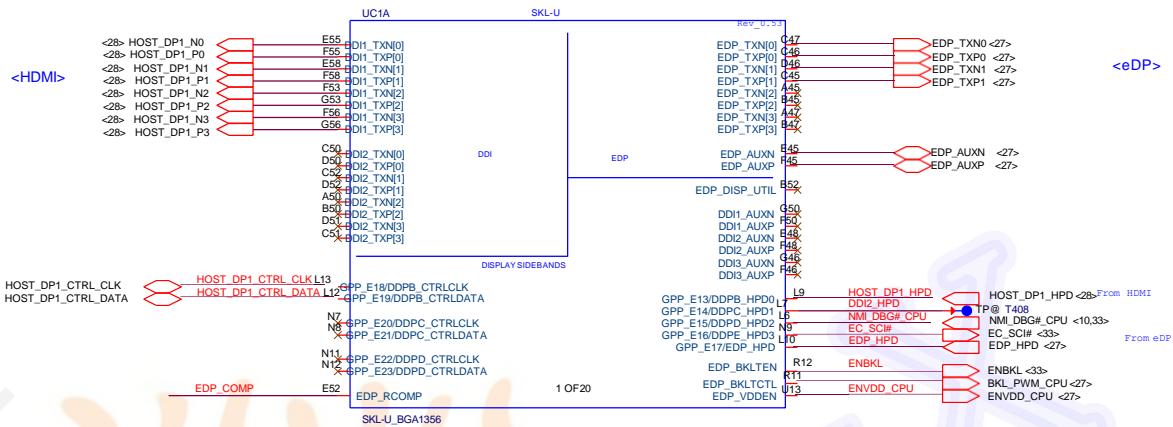
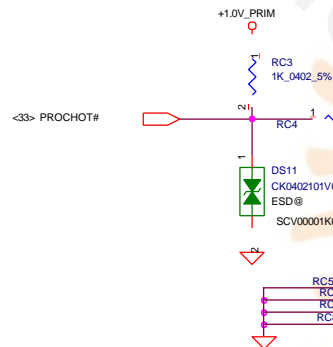
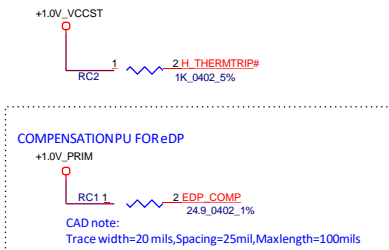
1 = Port B is detected.

SOC_DP2_CTRL_DATA (Internal Pull Down):

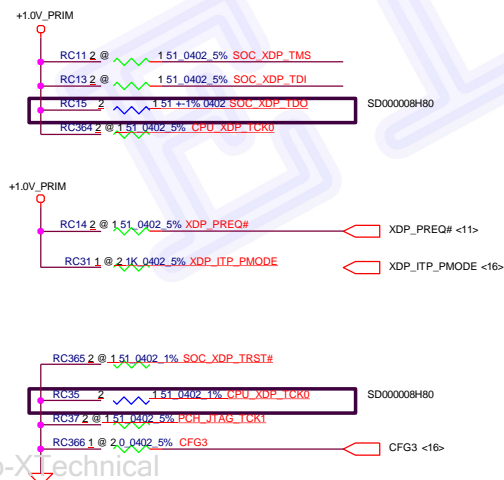
Display Port C Detected

0 = Port C is not detected.

1 = Port C is detected.

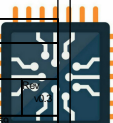


XDP CONN




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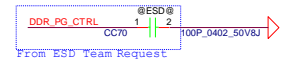
Title		Compal Electronics, Inc.	
		SKL-U(1/12)DDI,MSIC,XDP,EDP	
Document Number		CSL50 LA-E791P	
Date		Friday, January 05, 2018	
Sheet		5 of 5	

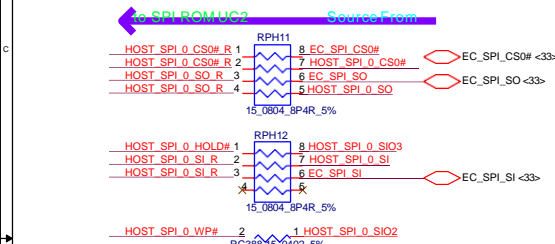


Eletro-X

Electro-XTechnical07

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<p>DATE: Friday, January 05, 2018</p>			<p>Sheet 6</p>	<p>of 59</p>





UC2

HOST_SPI_0_CS#_R 1

HOST_SPI_0_SO_R 2

HOST_SPI_0_WP#_R 3

CS# 1

DO(I/O) HOLD#(I/O) 2

WP#(I/O2) 3

GND 4

VCC 5

CLK 6

DI(I/O) 7

8

HOST_SPI_0_HOLD#_R

HOST_SPI_0_CLK_R

HOST_SPI_0_SI_R

121H 0201 10V6K

XM2SQH64AHG SOP 8P

ACES_91960-008AL_8P-1

Use socket footprint

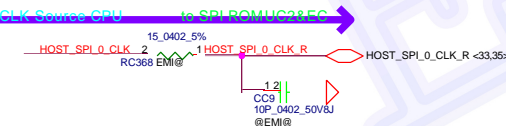
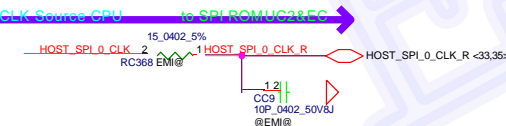
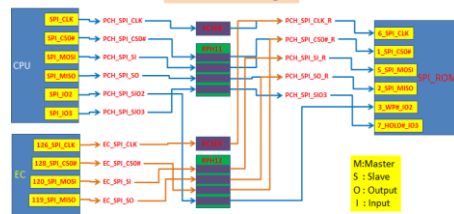


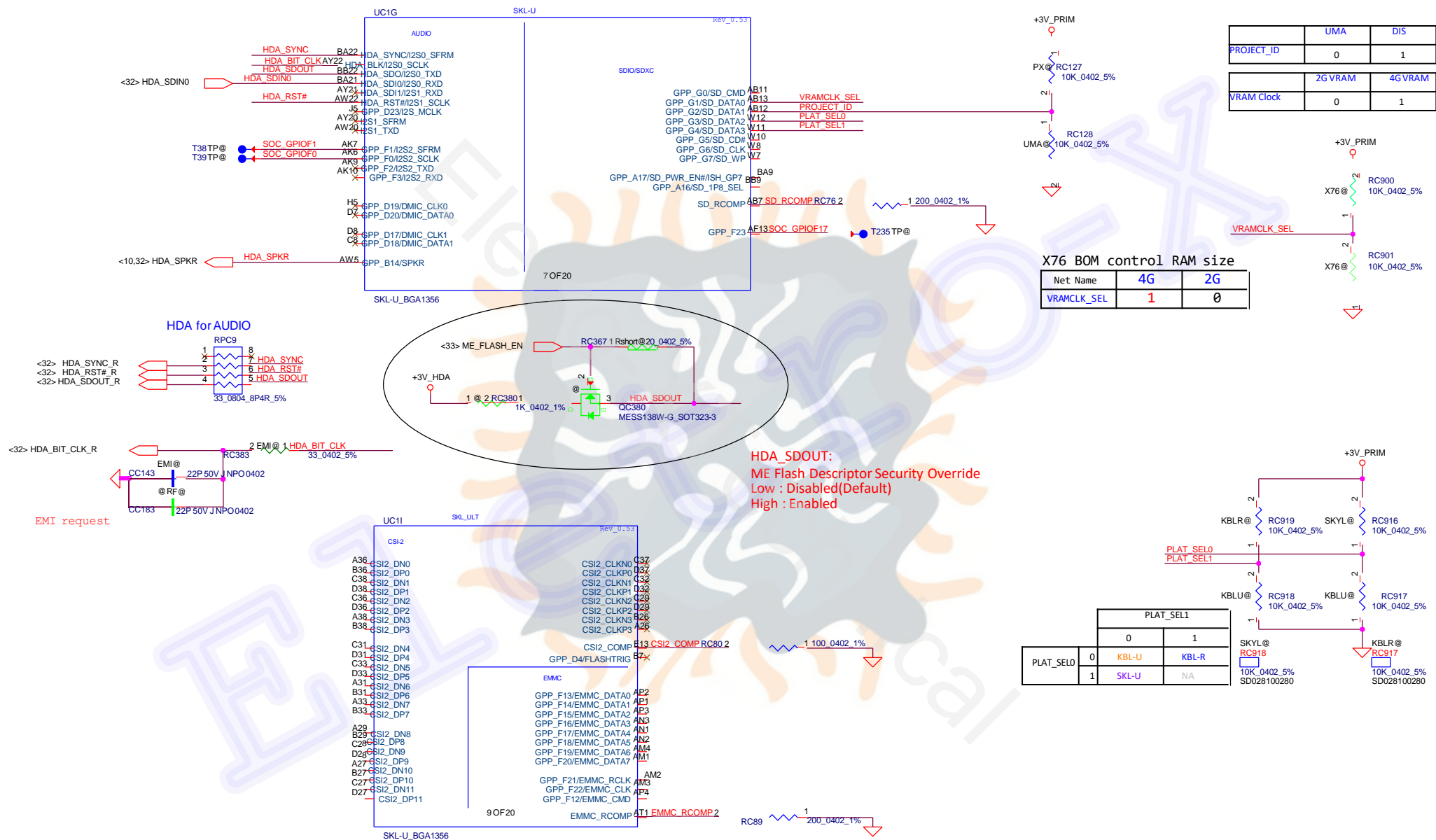
Figure 1: Block diagram of the proposed system architecture. The diagram illustrates the data flow between a CPU, an FC (Fuzzy Controller), and two intermediate processing blocks (SPI_C1 and SPI_S1) before reaching the final output block (SPI_R).

Legend:

- M: Master
- S: Slave
- O: Output
- I: Input



Title			
SKL-U(3/12)SPI,ESPI,SMB,LPC			
Document Number			
CSL50 LA-E791P			
Printer	Editor	January 05, 2018	Sheet 7 of 7



	UMA	DIS
PROJECT_ID	0	1

	2G VRAM	4G VRAM
VRAM Clock	0	1

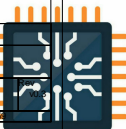
Net Name	4G	2G
VRAMCLK_SEL	1	0

		PLAT_SEL1	
		0	1
PLAT_SELO	0	KBL-U	KBL-R
	1	SKL-U	NA

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Issued Date	2017/04/10	Deciphered Date	2019/12/15


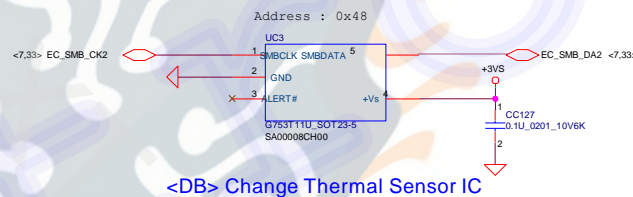
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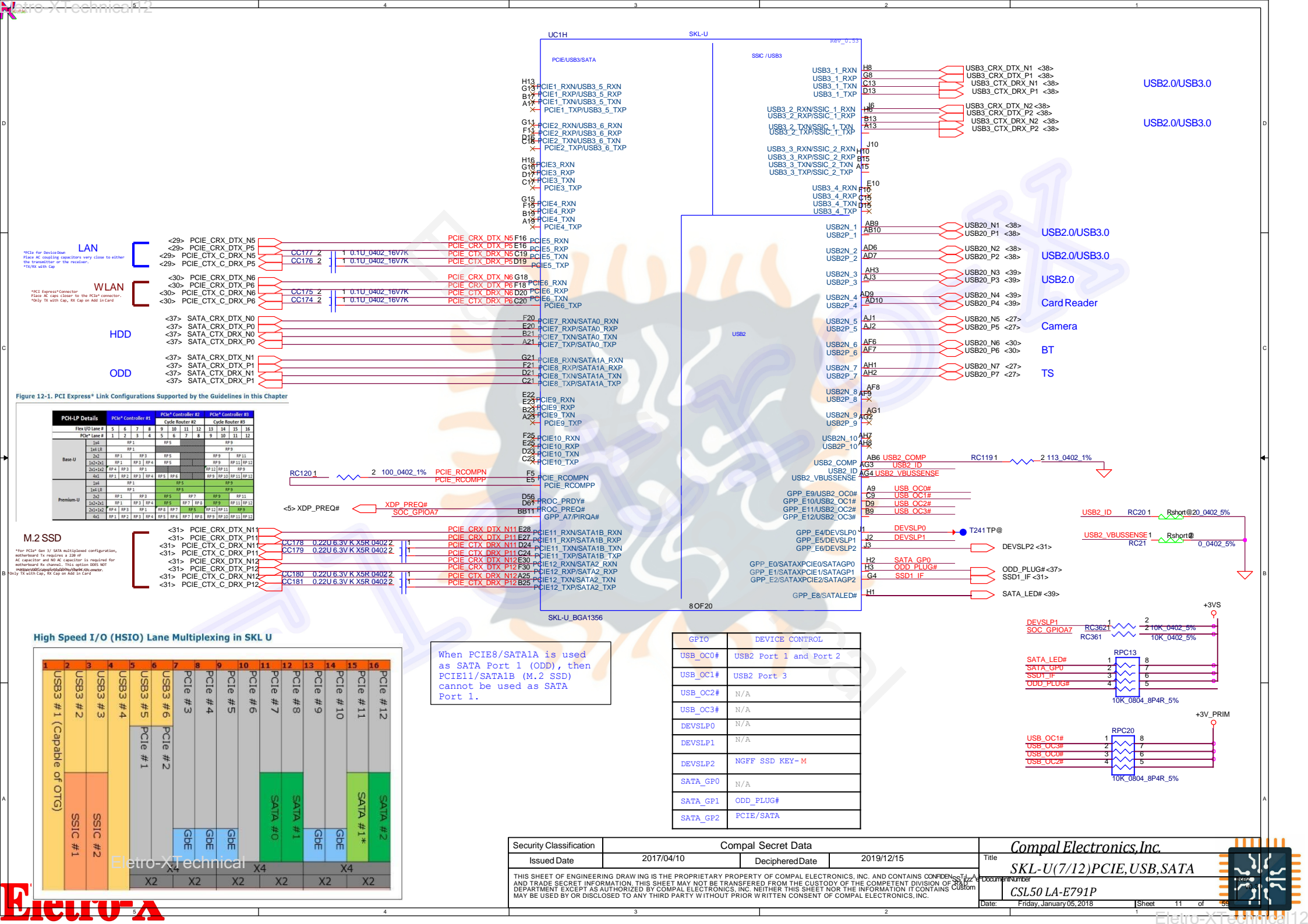
Title		Compal Electronics, Inc.	
Document Number		SKL-U(4/12)HDA,EMMC,SDIO,CS	
Date		CSL50 LA-E791P	
Date		Friday, January 05, 2018	
Sheet		8 of 99	



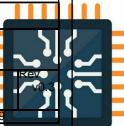


1 = LPC Mode



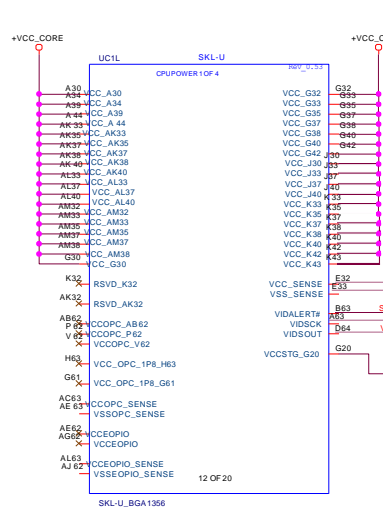


Eleto-XTechnical

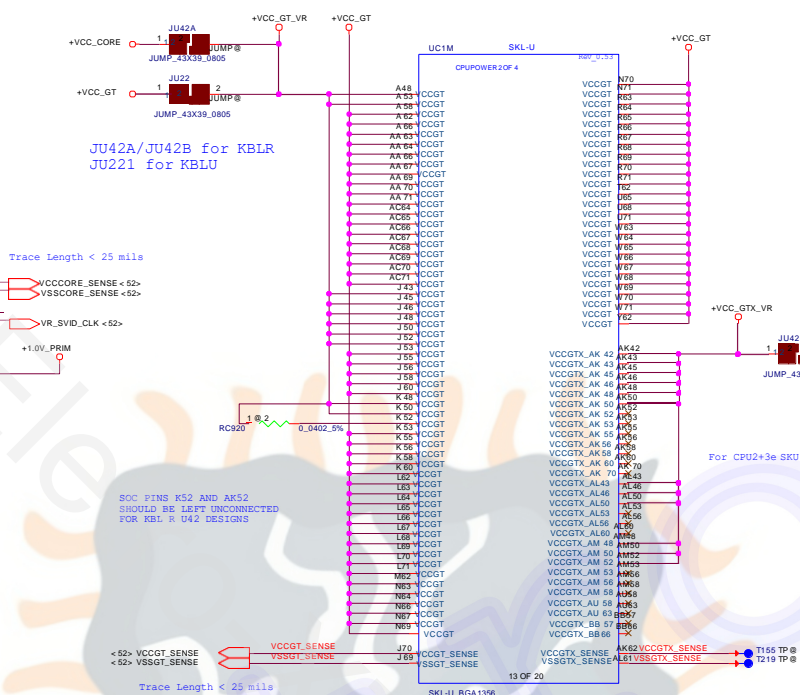
Fleuro-XTechnical1



For CPU2+3e SKU

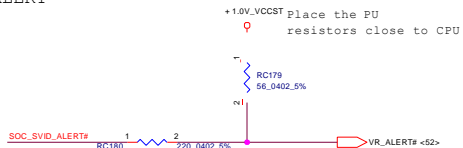


Trace Length < 25 mils



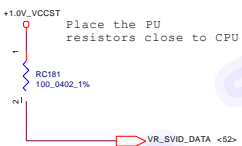
For CPU2+3e SKU

SVID ALERT



(To VR)

SVD DATA

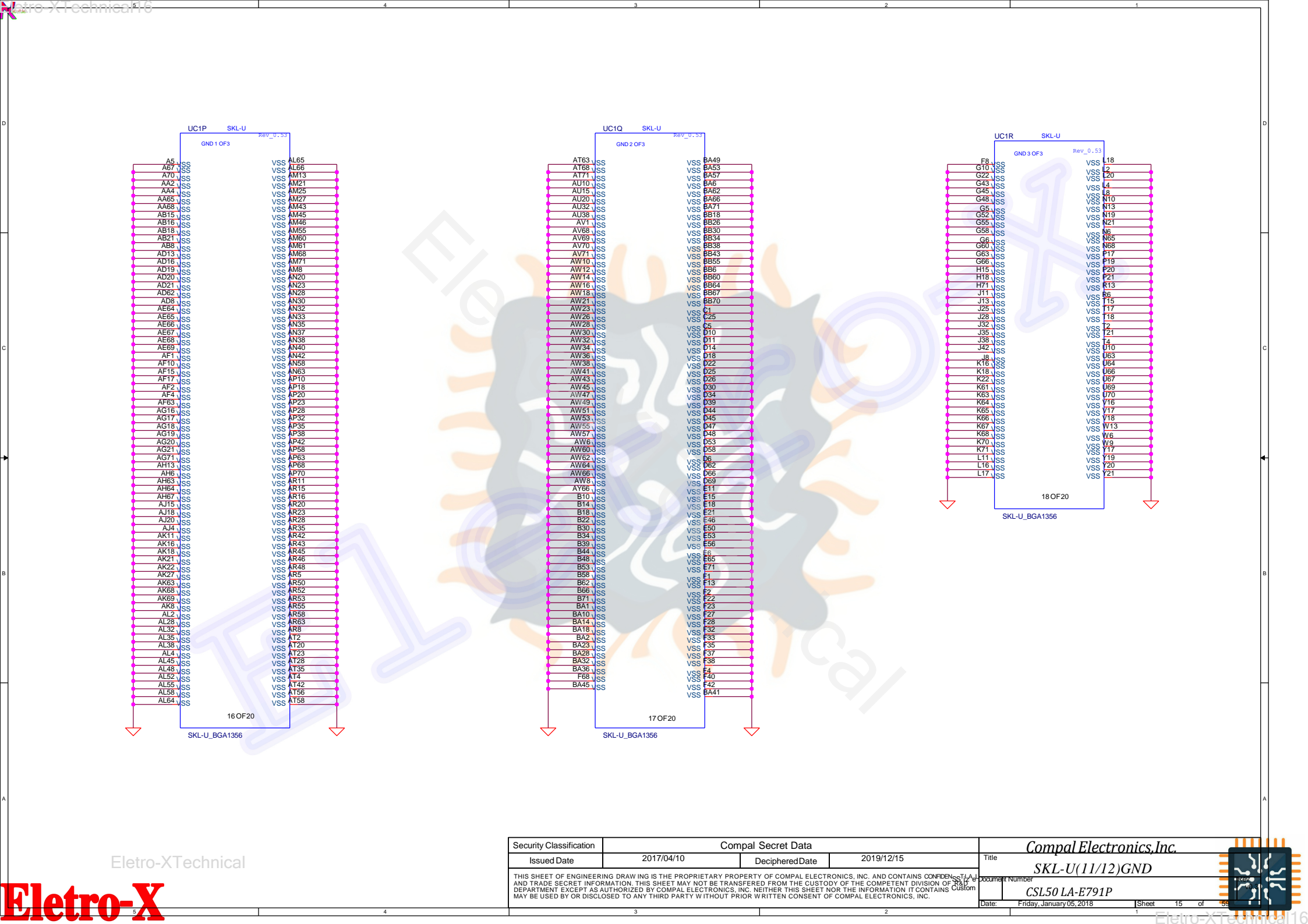


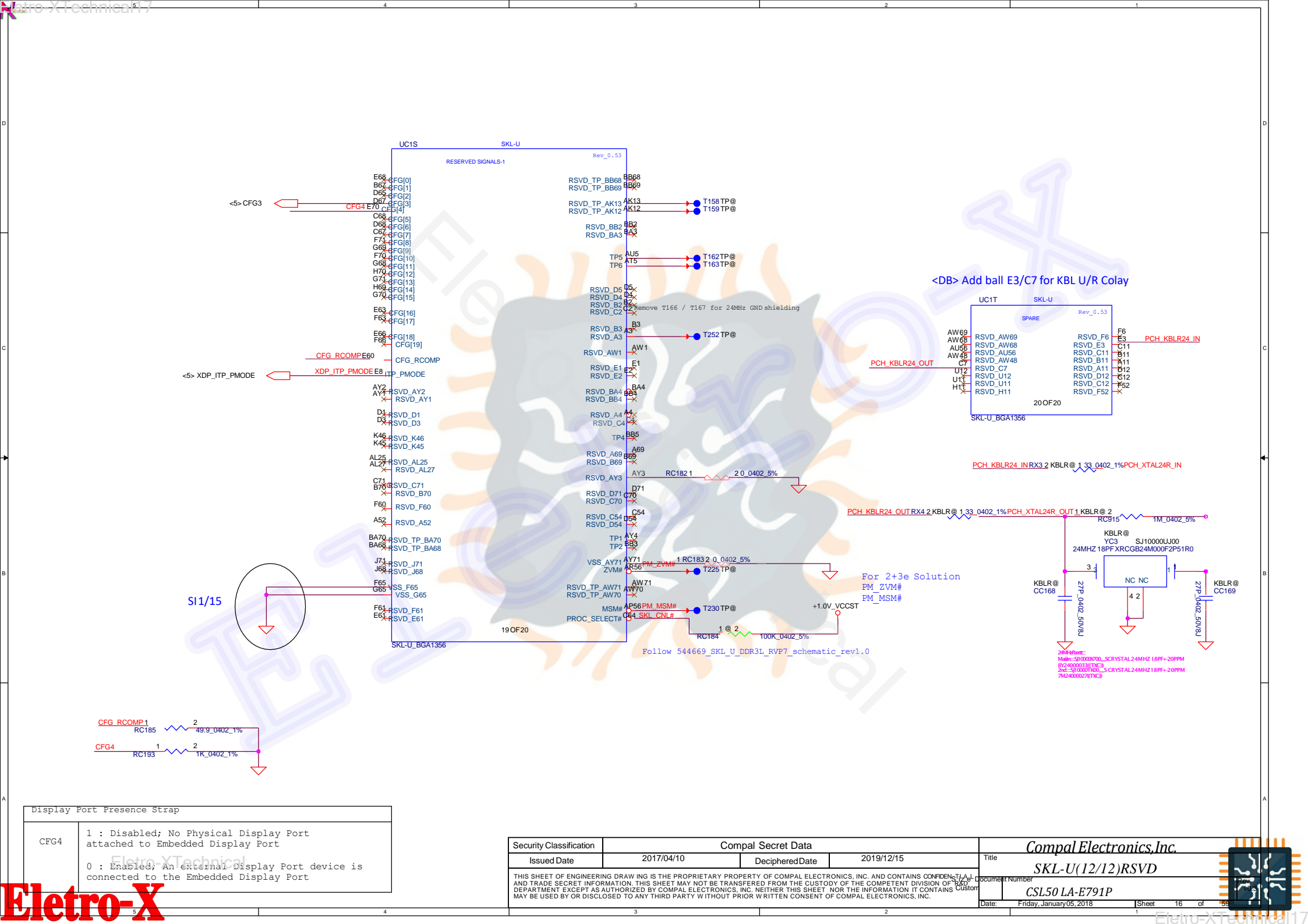
(To VR)

Ball #	Ball Names R-U42	Ball Names U22	R-U42/U22 common board guidelines
C7	XTAL24_OUT	NC	connect to R-U42 XTAL24_OUT
E3	XTAL24_IN	NC	connect to R-U42 XTAL24_IN
E35	NC	XTAL24_OUT	connect to U22 XTAL24_OUT
E37	NC	XTAL24_IN	connect to U22 XTAL24_IN
AK42	VCCCORE	VccGTx	connect to VccGTx/VCCCORE power plane island
AK43	VCCCORE	VccGTx	
AK45	VCCCORE	VccGTx	
AK46	VCCCORE	VccGTx	
AK48	VCCCORE	VccGTx	
AK50	VCCCORE	VccGTx	
AL43	VCCCORE	VccGTx	
AL46	VCCCORE	VccGTx	
AL50	VCCCORE	VccGTx	
AM48	VCCCORE	VccGTx	
AM50	VCCCORE	VccGTx	connect to VccGTx/VCCCORE power plane island
AM52	VCCCORE	VccGTx	
J43	VCCCORE	VCCGT	
J45	VCCCORE	VCCGT	
J46	VCCCORE	VCCGT	
J48	VCCCORE	VCCGT	
J50	VCCCORE	VCCGT	
J52	VCCCORE	VCCGT	
K48	VCCCORE	VCCGT	
K50	VCCCORE	VCCGT	
A48	VCCCORE	VCCGT	Must Not Be Connected. RVP use this signal for debug and testing purpose only
A53	VCCCORE	VCCGT	
AK52	RSVD	VccGTx	
K52	RSVD	VCCGT	Must Not Be Connected. RVP use this signal for debug and testing purpose only

Must Not Be Connected. RVP use this signal for debug and testing purpose only

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Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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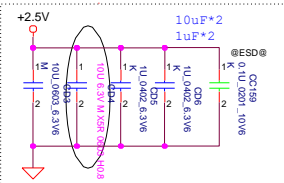
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Document Number		SKL-U(12/12)RSVD	
Date		Friday, January 05, 2018	
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Interleaved Memory

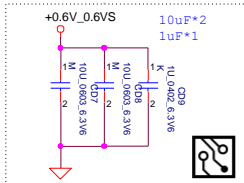
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Layout Note:
Place near JDIMM1.257,259

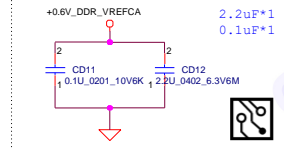
Layout Note:
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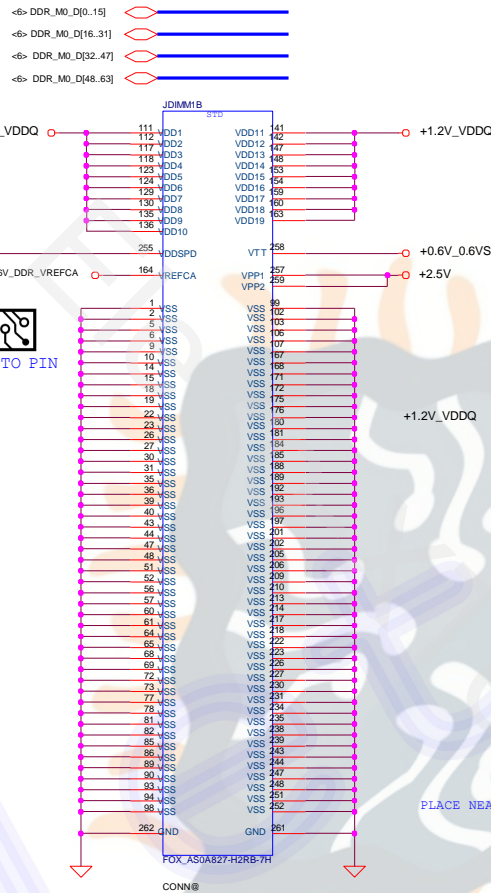
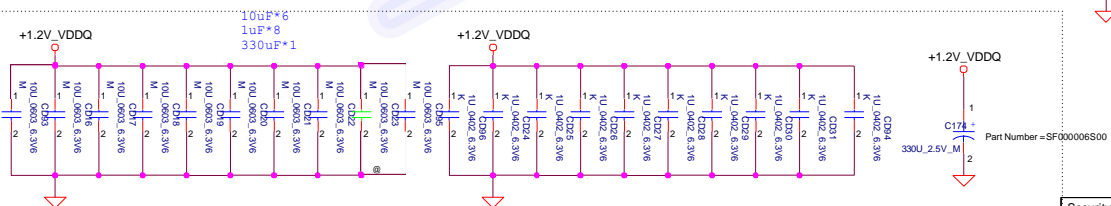
Layout Note:
PLACE THE CAP near JDIMM1. 164



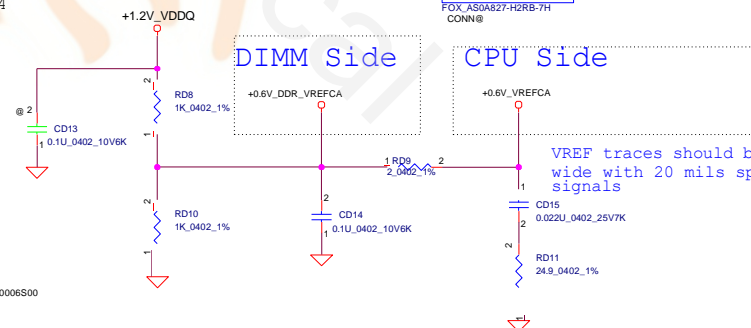
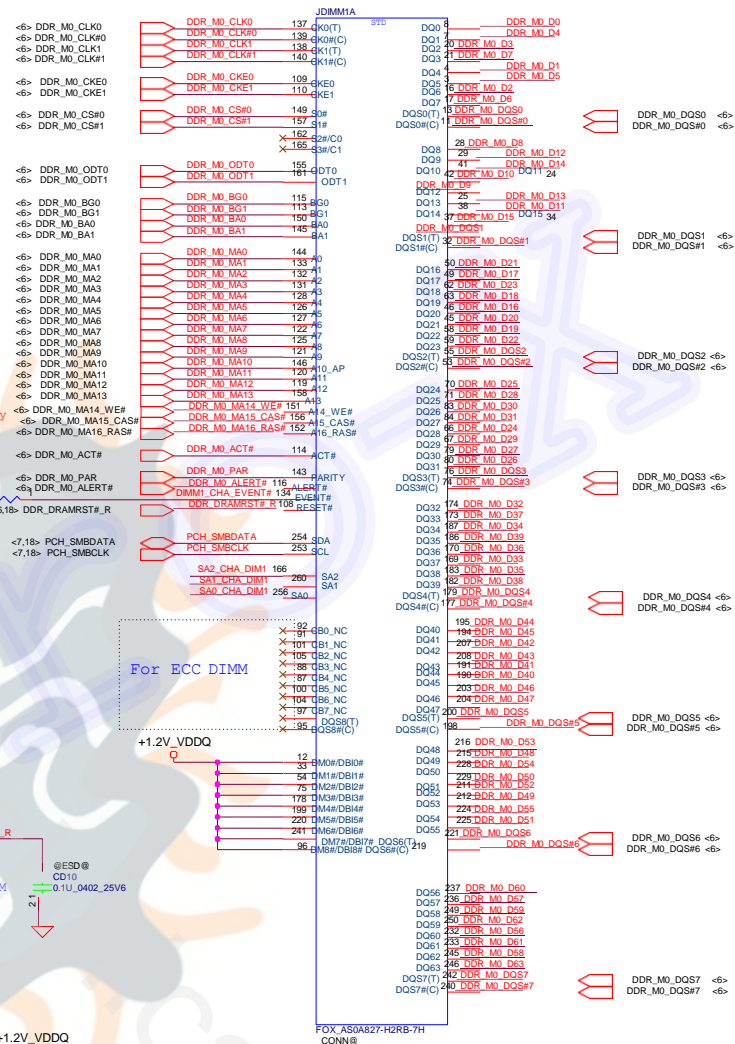
Layout Note:
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Layout Note:
Place near JDIMM1



Part Number:LTCX0069GA0
Part Value:S SOCKET FOX AS0A827-H2RB-7H 260P DDR4

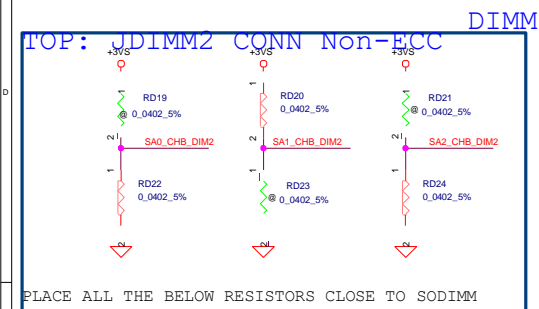


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				Sheet 17 of	

CHANNEL-B

Interleaved Memory

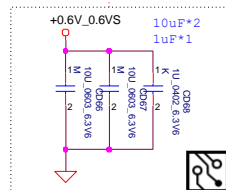
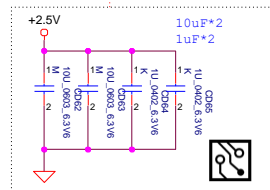
STD (5.2 mm)



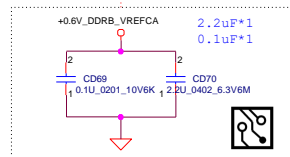
SPD ADDRESS FOR CHANNEL B :
 WRITE ADDRESS: 0XA4
 READ ADDRESS: 0XA3
 SA0 = 0; SA1 = 1; SA2 = 0.
 DDR4 POR OPERATING SPEED: 1867 MT/S
 STRETCH GOAL IS 2133 MT/S

Layout Note:
Place near JDIMM2.257,259

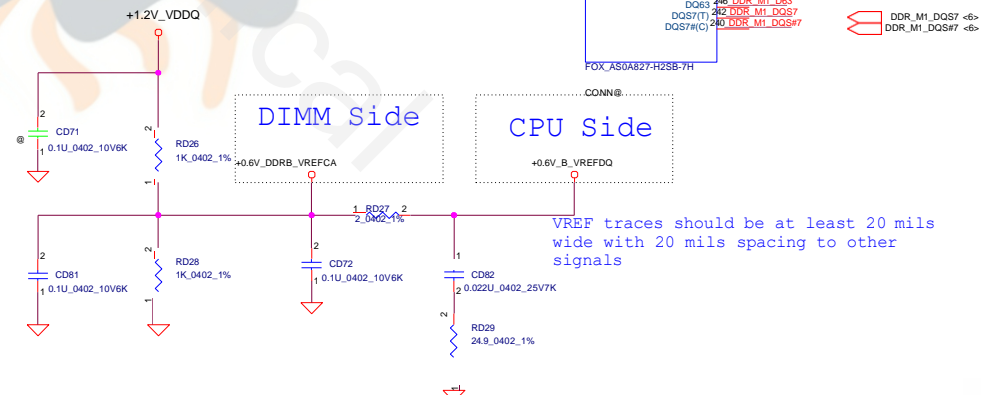
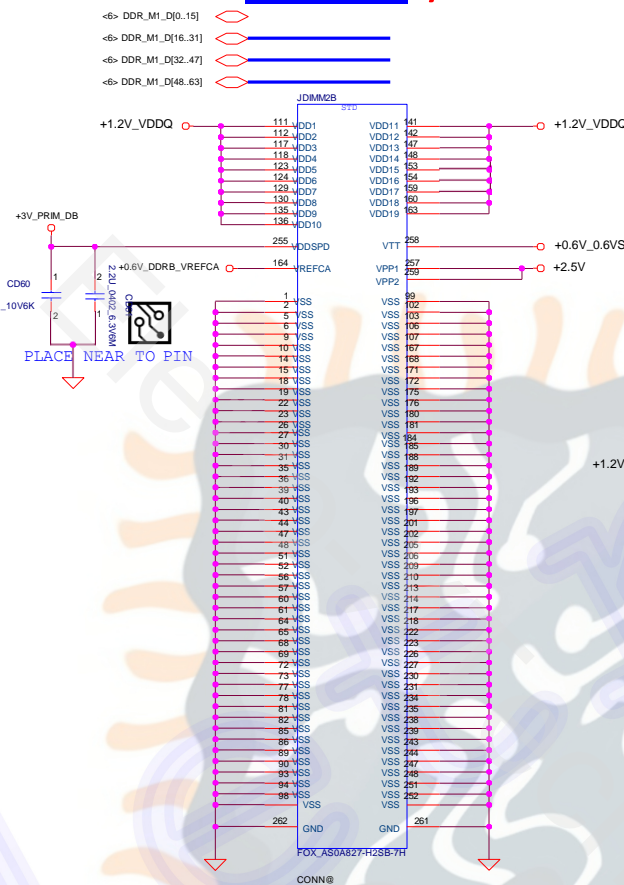
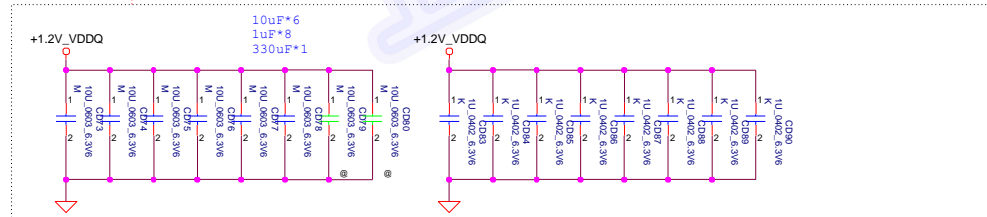
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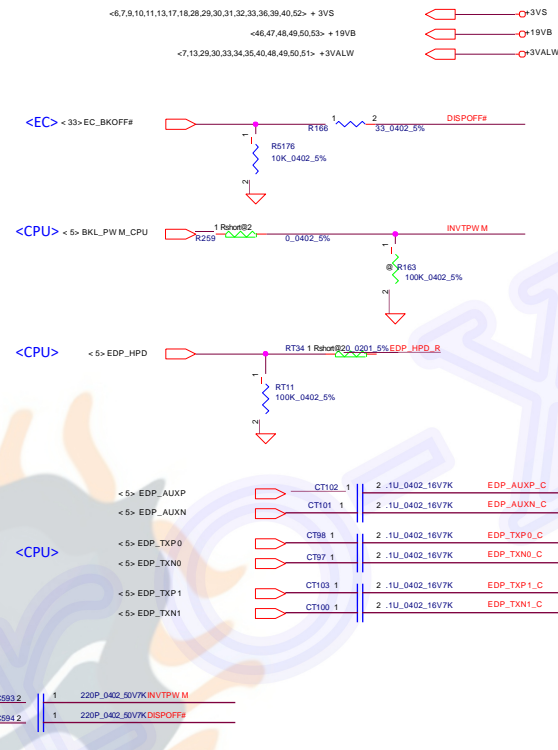
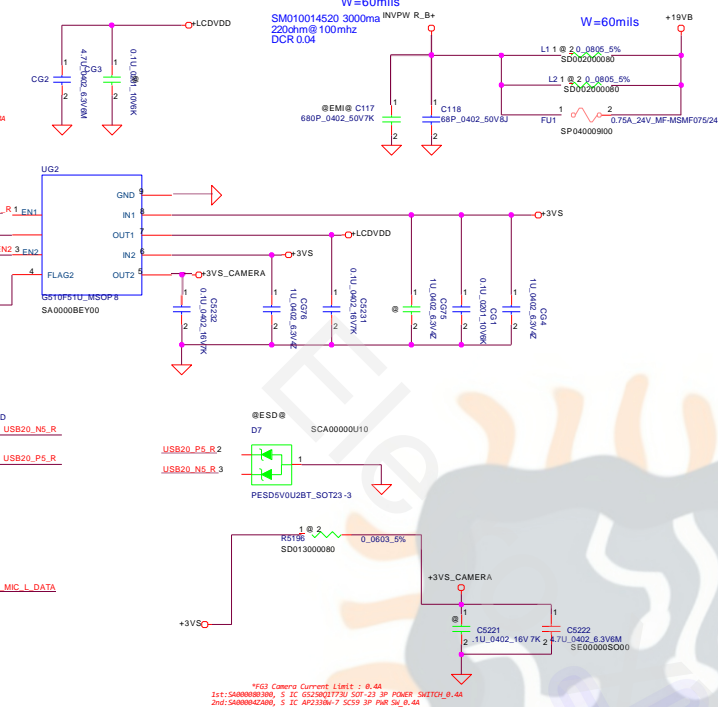
Layout Note:
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FROM THE JDIMM2



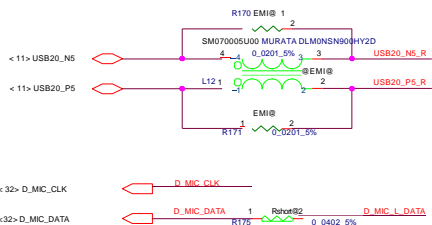
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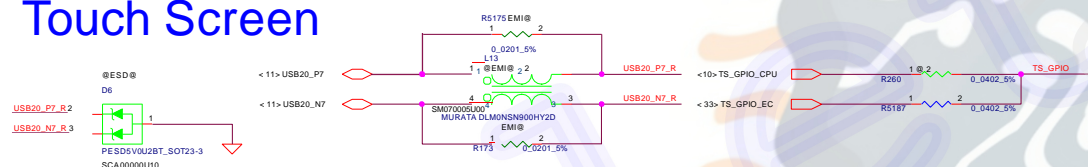
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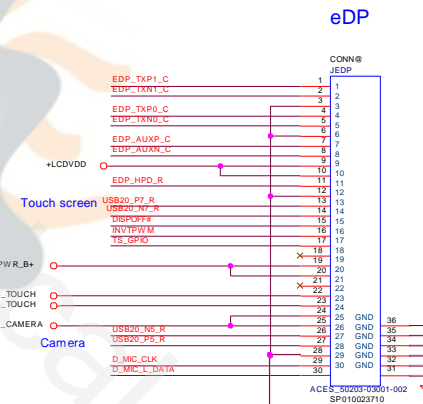
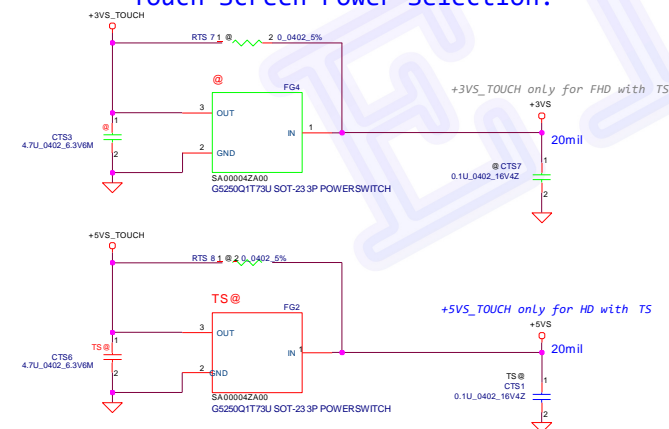
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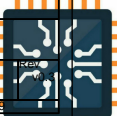
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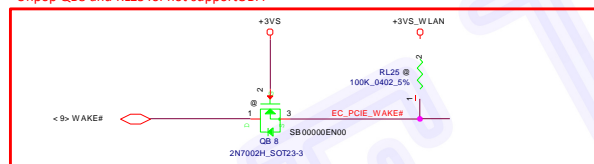


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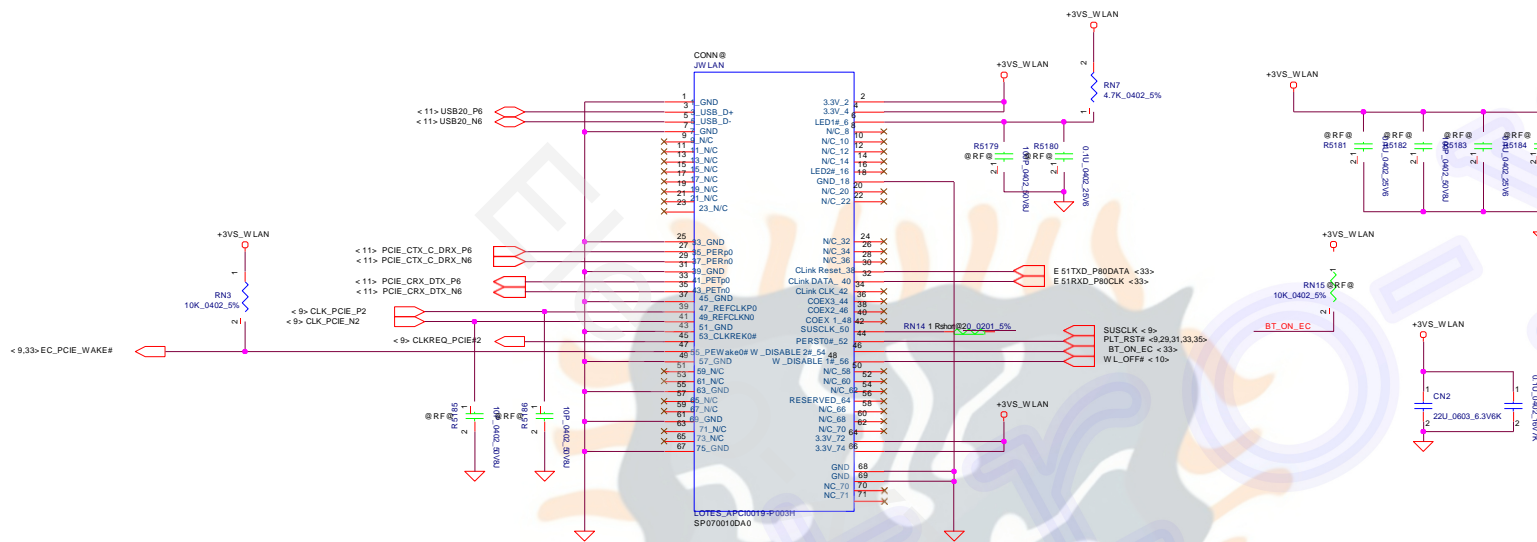
NGFF and WLAN

Unpop Q88 and RL25 for not supportOBFF

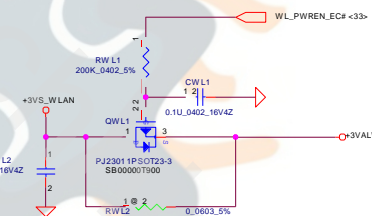


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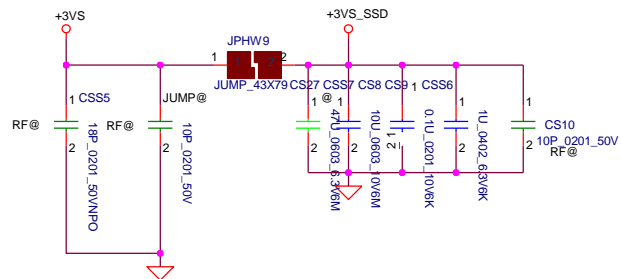
<7,13,29,33,34,35,40,48,49,50,51> +3VALW



ActiveLow



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				CSL50 LA-E791P
				Date: Friday, January 05, 2018



<6,7,9,10,11,13,17,18,27,28,29,30,32,33,36,39,40,52>

+3VS

+3VS

Figure 12-1. PCI Express® Link Configurations Supported by the Guidelines in this Chapter

PCH-LP Details	PCIe® Controller #1				PCIe® Controller #2				PCIe® Controller #3			
Flex I/O Lane #	5	6	7	8	9	10	11	12	13	14	15	16
PCIe® Lane #	1	2	3	4	5	6	7	8	9	10	11	12
Base-U	1x4	RP 1			RP 5			RP 9				
	1x4 LR	RP 1			RP 5			RP 9				
	2x2	RP 1	RP 3	RP 4	RP 5			RP 9				RP 11
	1x2+2x1	RP 1	RP 3	RP 4	RP 5			RP 9				RP 11
	2x1+1x2	RP 4	RP 3	RP 1	RP 5			RP 9				RP 11
Premium-U	4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6	RP 7	RP 8	RP 9	RP 10	RP 11
	1x4	RP 1			RP 5			RP 9				
	1x4 LR	RP 1			RP 5			RP 9				
	2x2	RP 1	RP 3	RP 4	RP 5			RP 9				RP 11
	1x2+2x1	RP 1	RP 3	RP 4	RP 5			RP 9				RP 11

<SSD>

<11> PCIe_CRX_DTX_N11

<11> PCIe_CRX_DTX_P11

<11> PCIe_CTX_C_DRX_N11

<11> PCIe_CTX_C_DRX_P11

<11> PCIe_CRX_DTX_P12

<11> PCIe_CRX_DTX_N12

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<11> PCIe_CTX_C_DRX_P12

<9> CLK_PCIE_N4

<9> CLK_PCIE_P4

SSD1_IF PU on CPU side RPC13.3 10K

@ RS21

100K_0402_5%

<11> SSD1_IF

@EMI @ CS16

VARIST_CK0402101V050402

SSD_PDET

+3VS

RS22

10K_0402_5%

Q51 SB000009Q80

2N7002KW_SOT323-3

pre PV: change to 10K for redriver detect pin voltage level

36.3.2.4 AC Capacitor General Guidelines for M.2 SSD Storage Routing on SATA / PCI Express® Multiplexed Ports

The following table summarizes the AC capacitor requirements on the motherboard when using the SATA/PCIe® multiplexed ports.

Note:

When SATA and PCIe® are muxed, always route according to SATA design guidelines. SATA does not support signal polarity reversal and does not support lane reversal.

39	GND	PCIMVMe_0090000NU90_MZVLW1T0HMLH-000H1_F73H1Q_00V1	39	GND	Return Current Path	40	GND	Return Current Path
41	PETn0	PCIe TX	42	N/C		43	TXP	Transmitter Differential Signal Pair
43	PETn1	PCIe TX	44	N/C		45	TXN	Transmitter Differential Signal Pair
45	GND	Return current path	46	N/C		47	GND	Return Current Path
47	PERn0	PCIe Rx	48	N/C		49	PERn1	Receiver Differential Signal Pair
49	PERn1	PCIe Rx	50	PERST#		51	GND	Return Current Path
51	GND	Return current path	52	CLKREQ#		53	GND	Return Current Path

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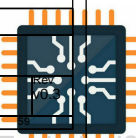
Compal Electronics, Inc.

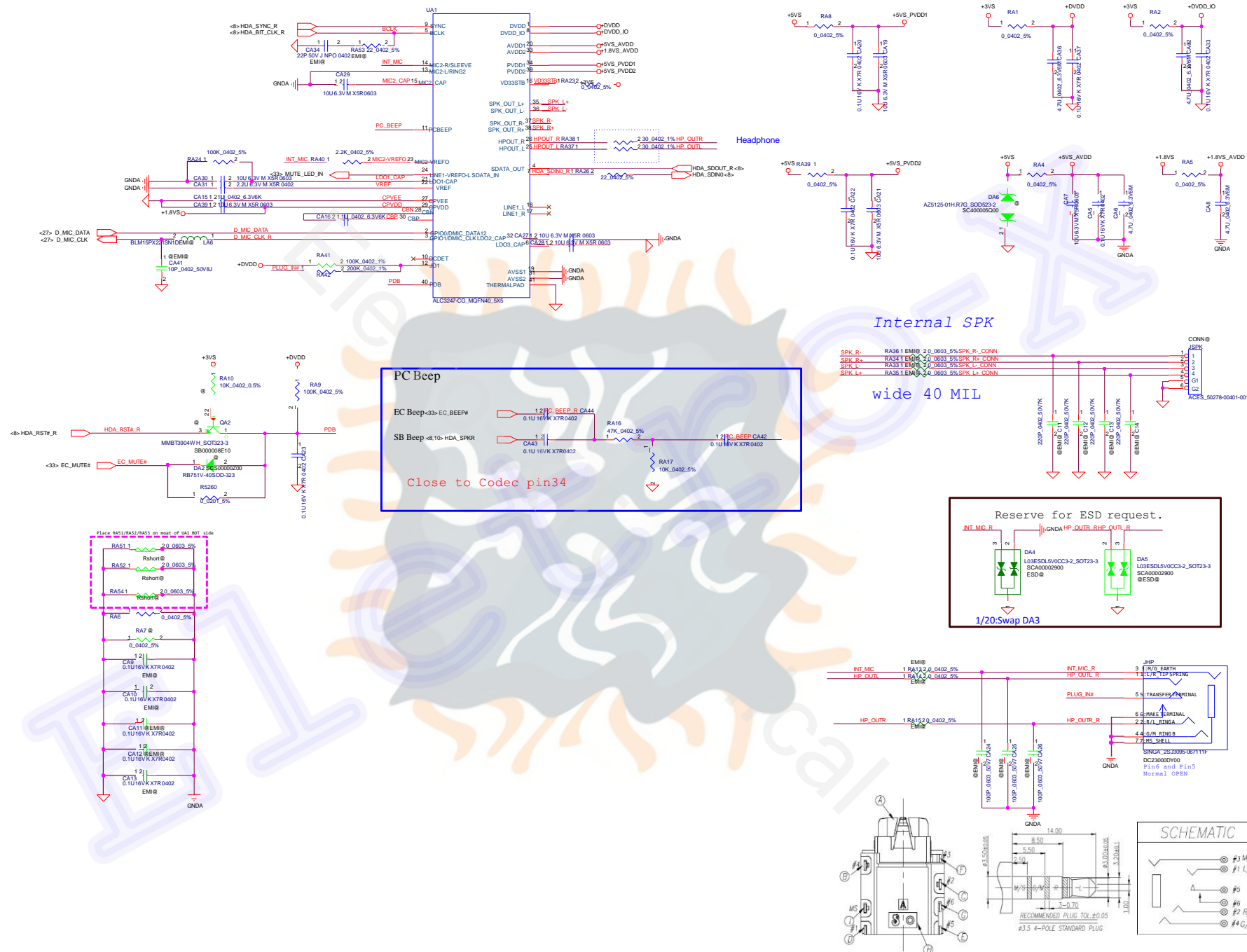
Title
M.2SSDDocument Number
CSL50 LA-E791P

Date: Friday, January 05, 2018

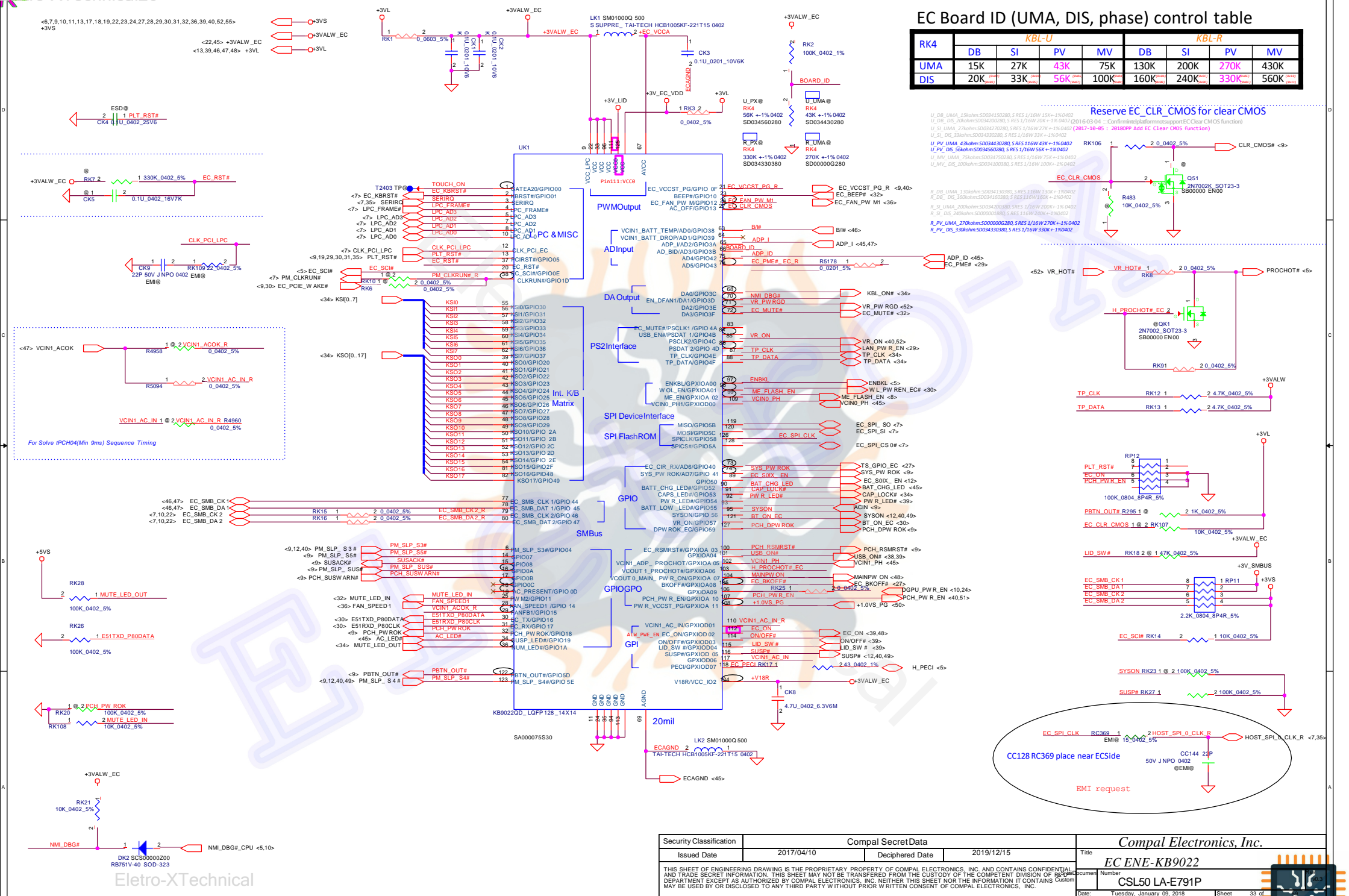
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Eletro-X Technical

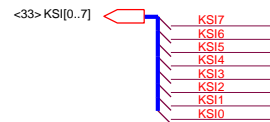
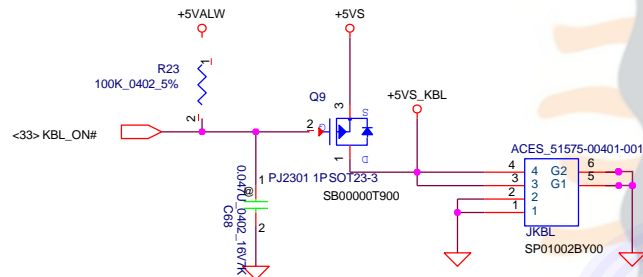
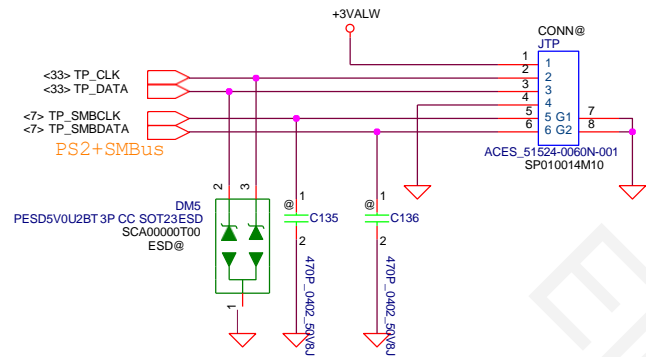




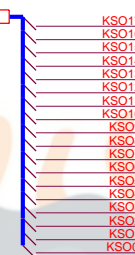
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TP Button BD Connector

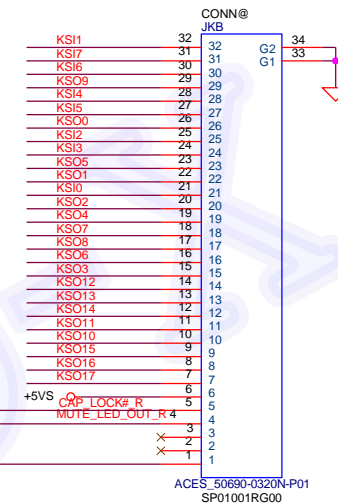


<33> KSO[0..17]



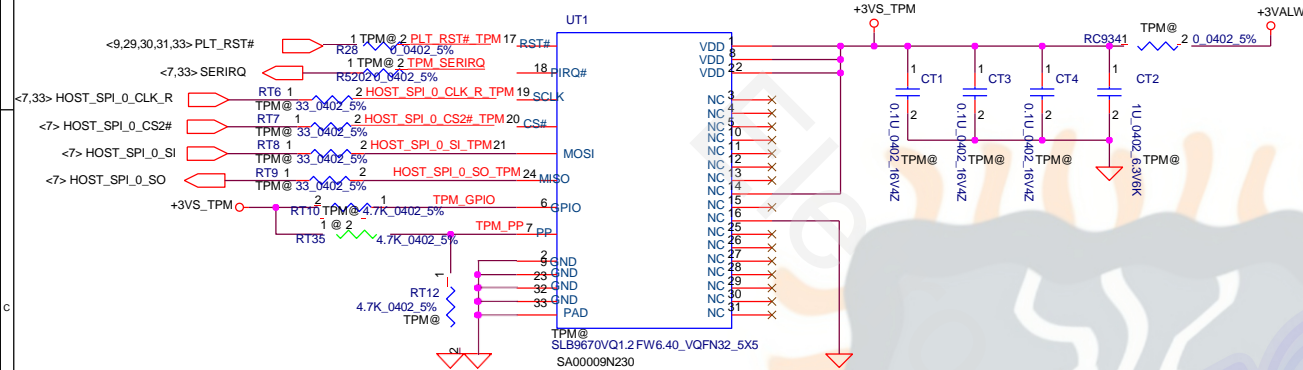
Pin1	Pin32	KB Spec
KSI1	5V	5V

Keyboard conn

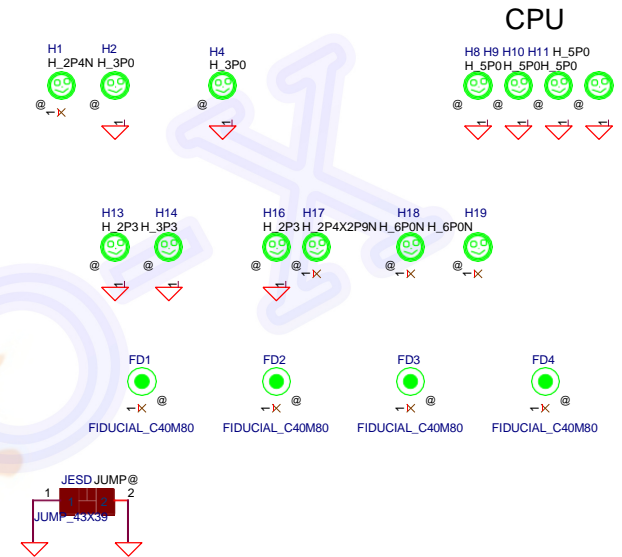


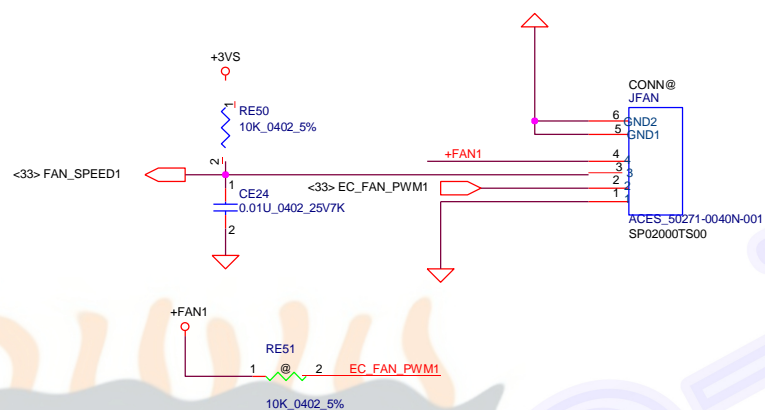
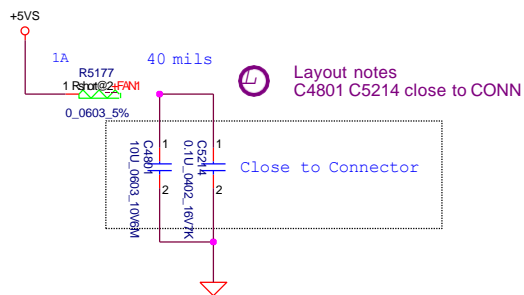
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TPM2.0



Screw Hole



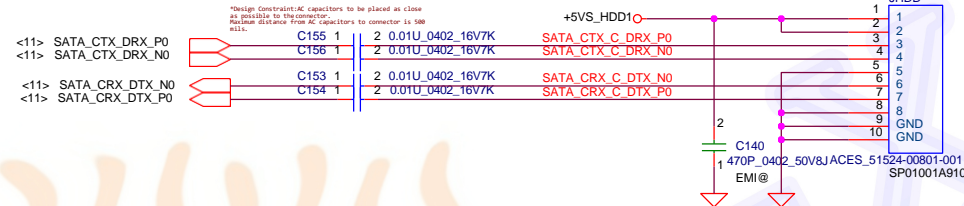
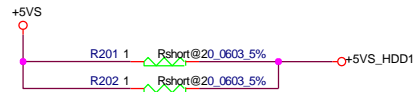


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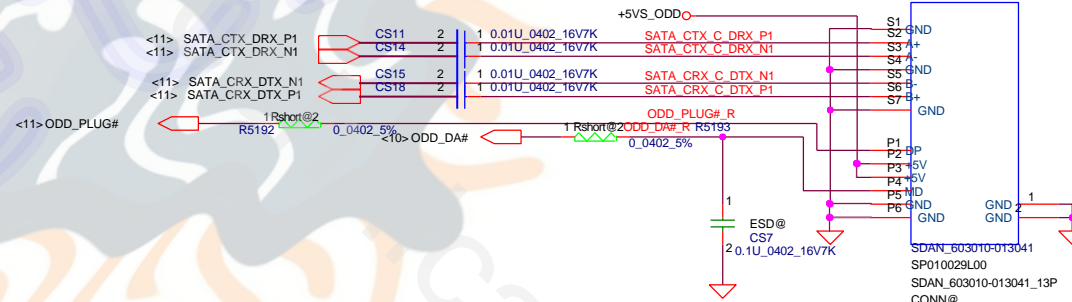
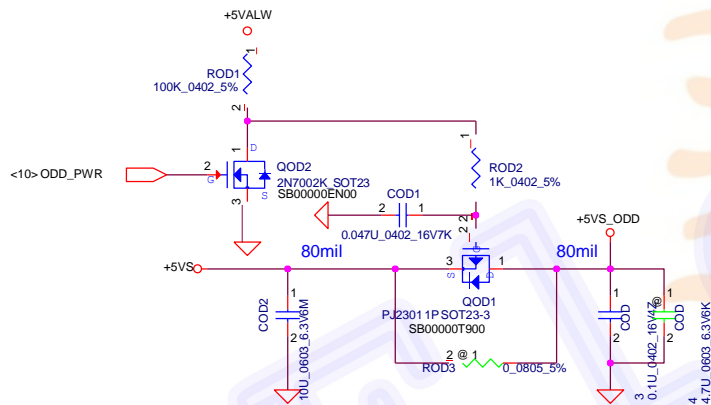
2.5" SATA HDD

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 <12,34,38,39,40,48,49,52,53> +5VALW
 <7,13,29,30,33,34,35,40,48,49,50,51> +3VALW

<PV> change short pad



SATA ODD

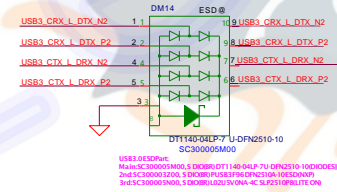
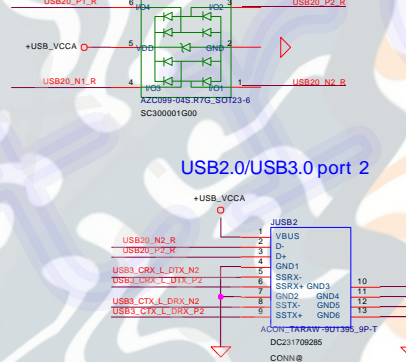
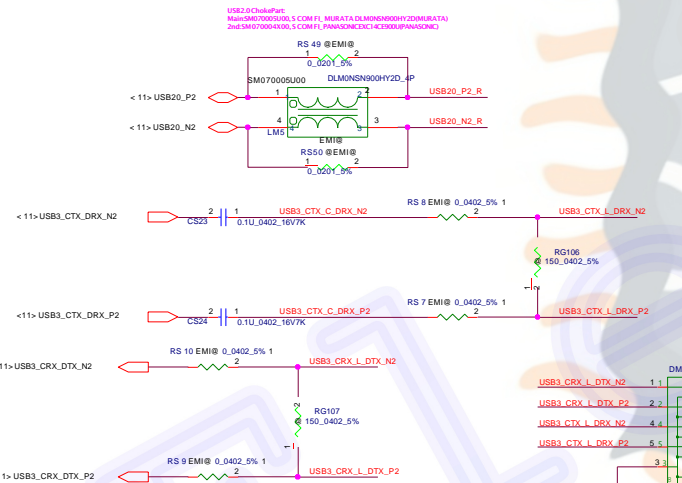
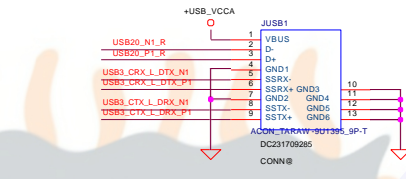
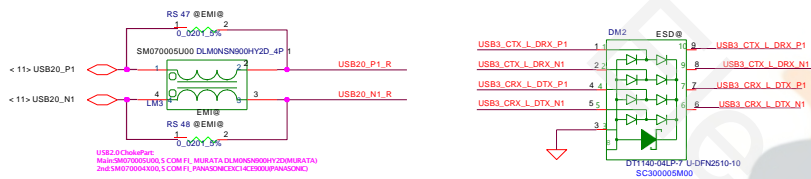
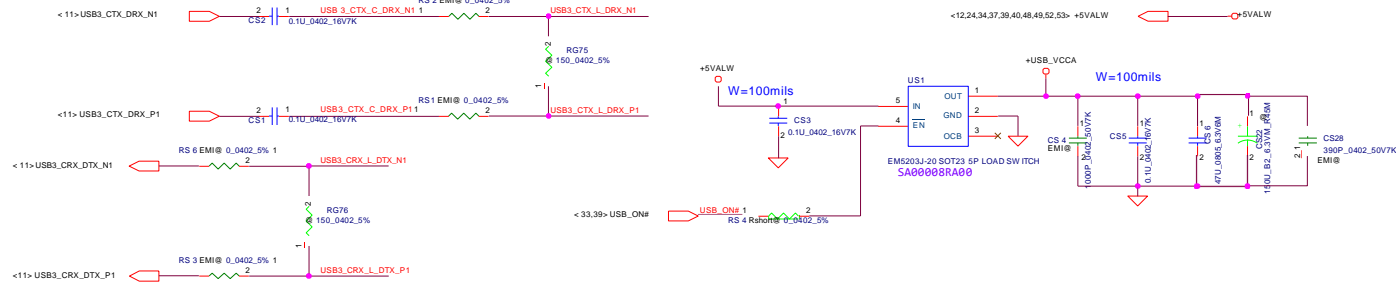


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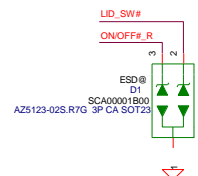
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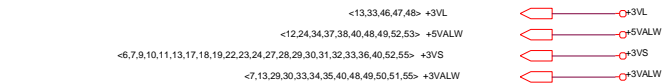
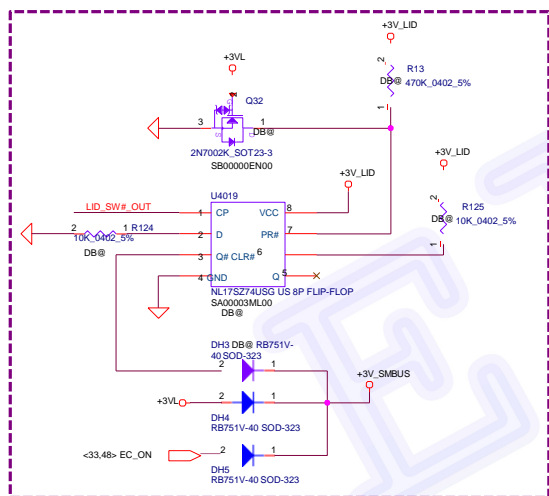
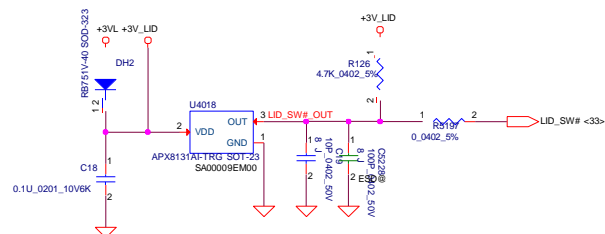




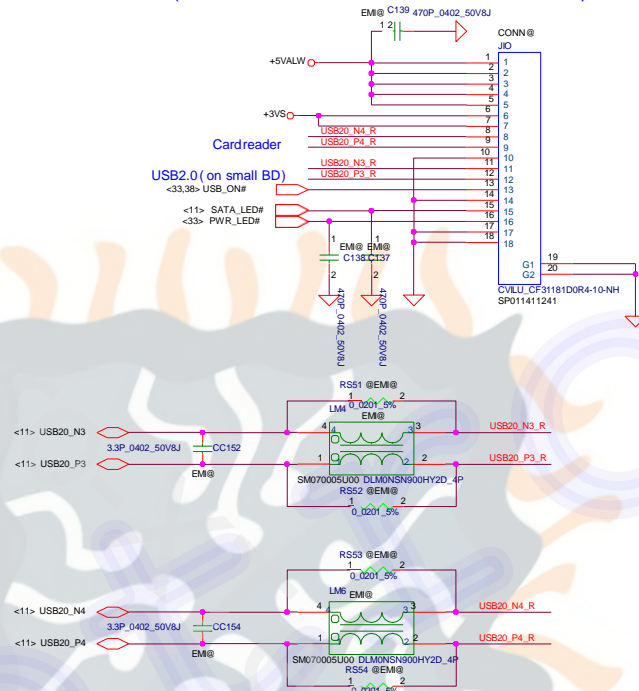
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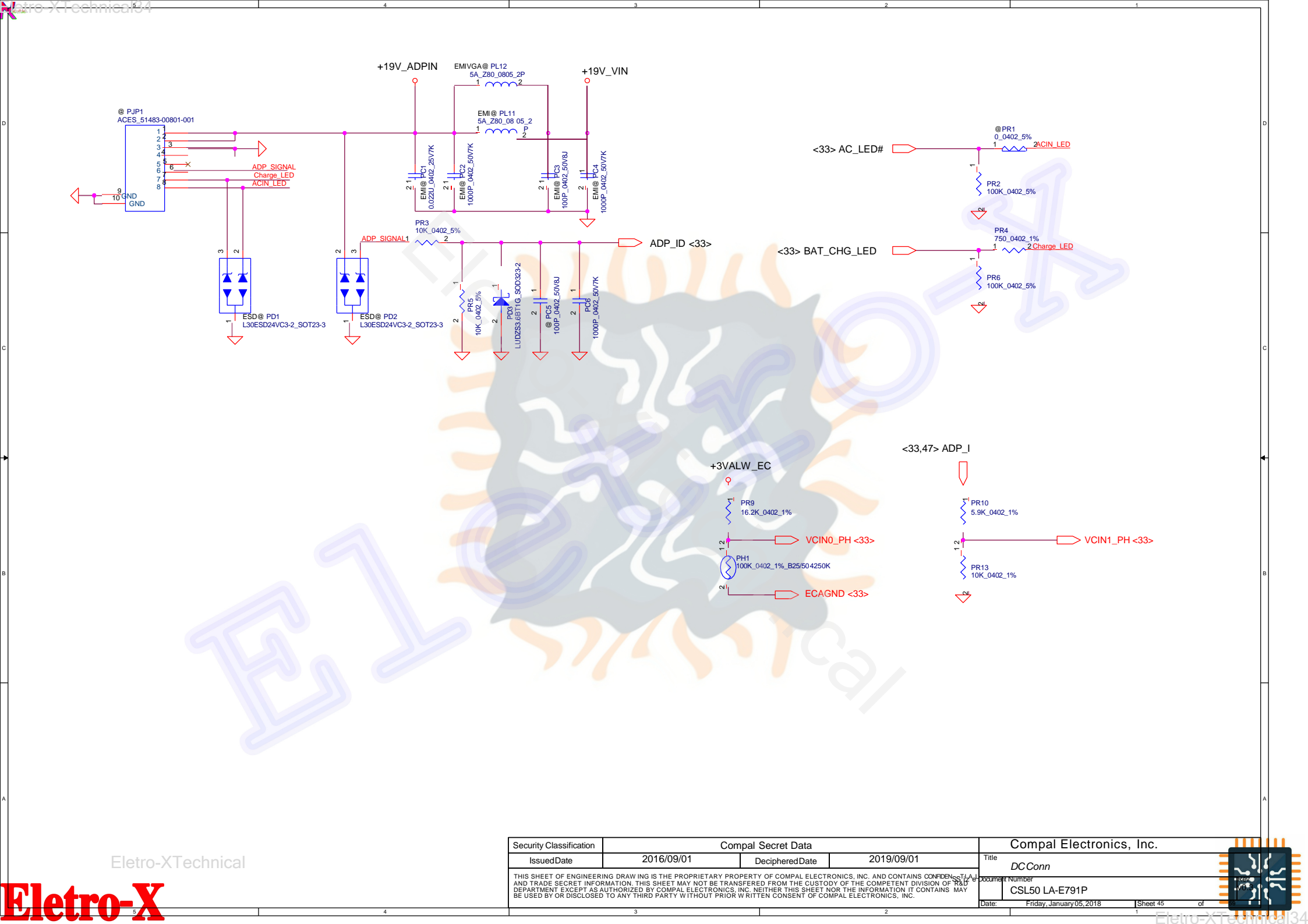
Lid Switch (Hall Effect Sensor)



IO BD Connector (USB2.0,Card reader,HDD & PWR LED)

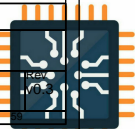


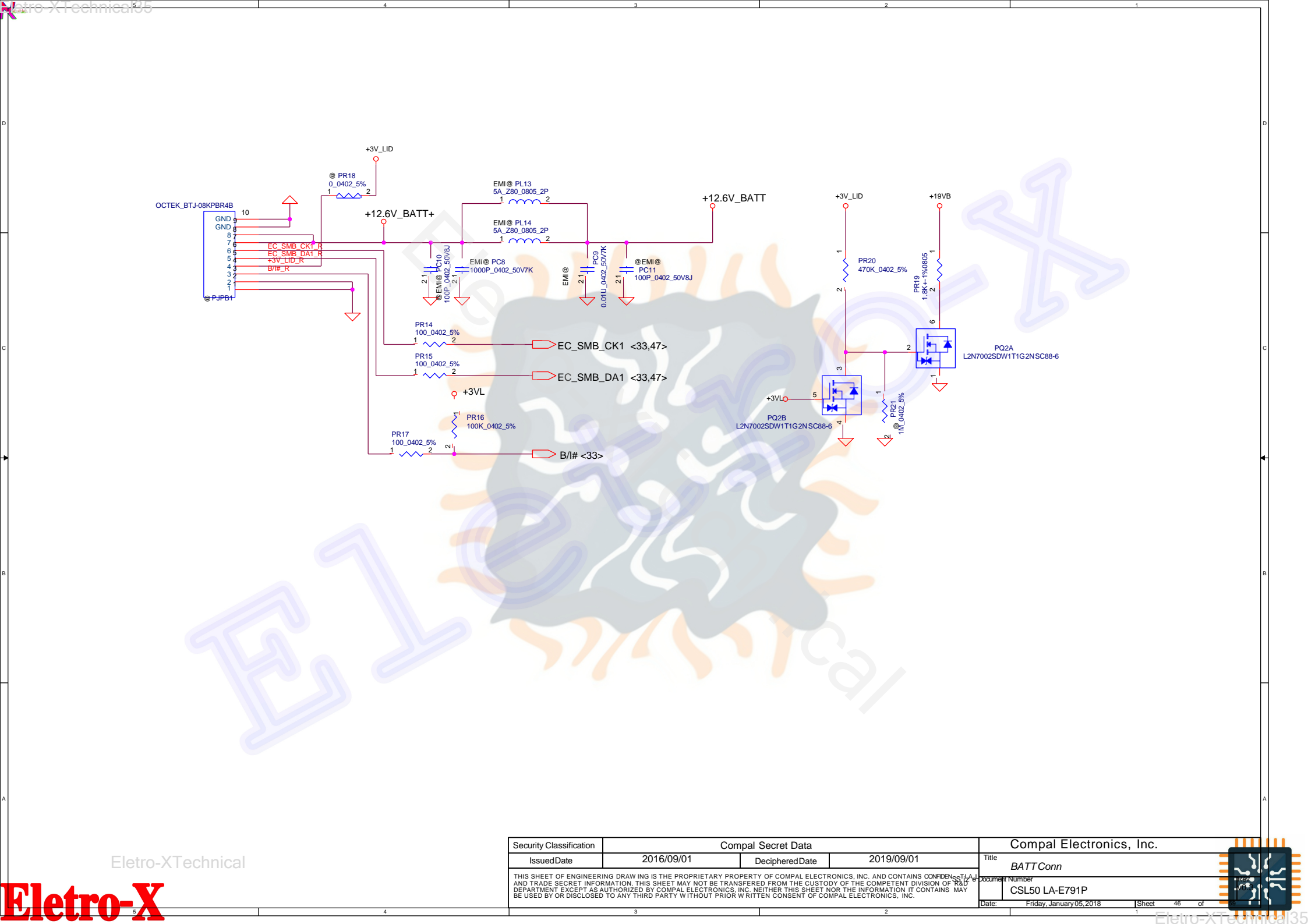
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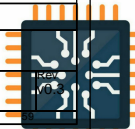
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Date	Friday, January 05, 2018
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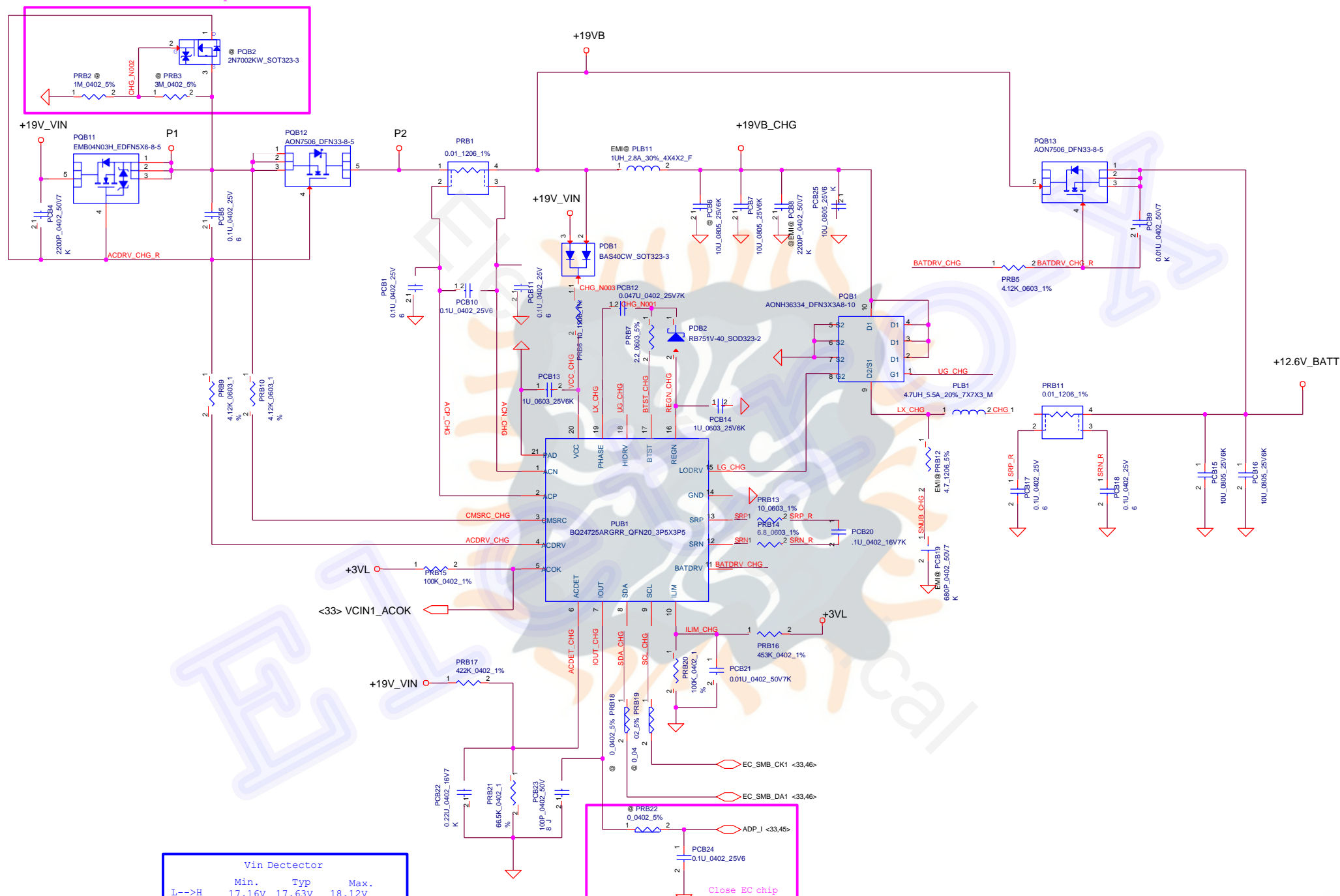


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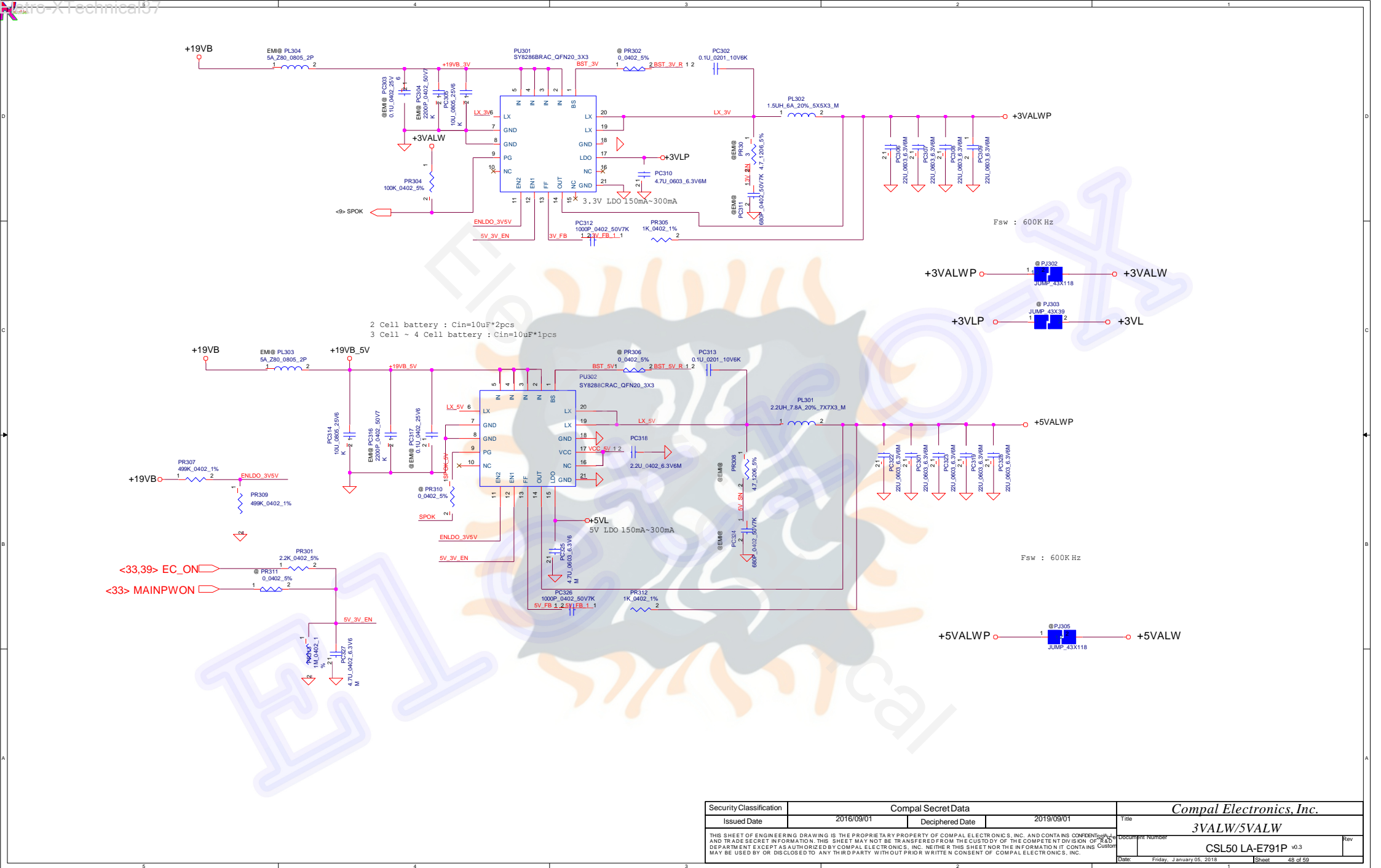
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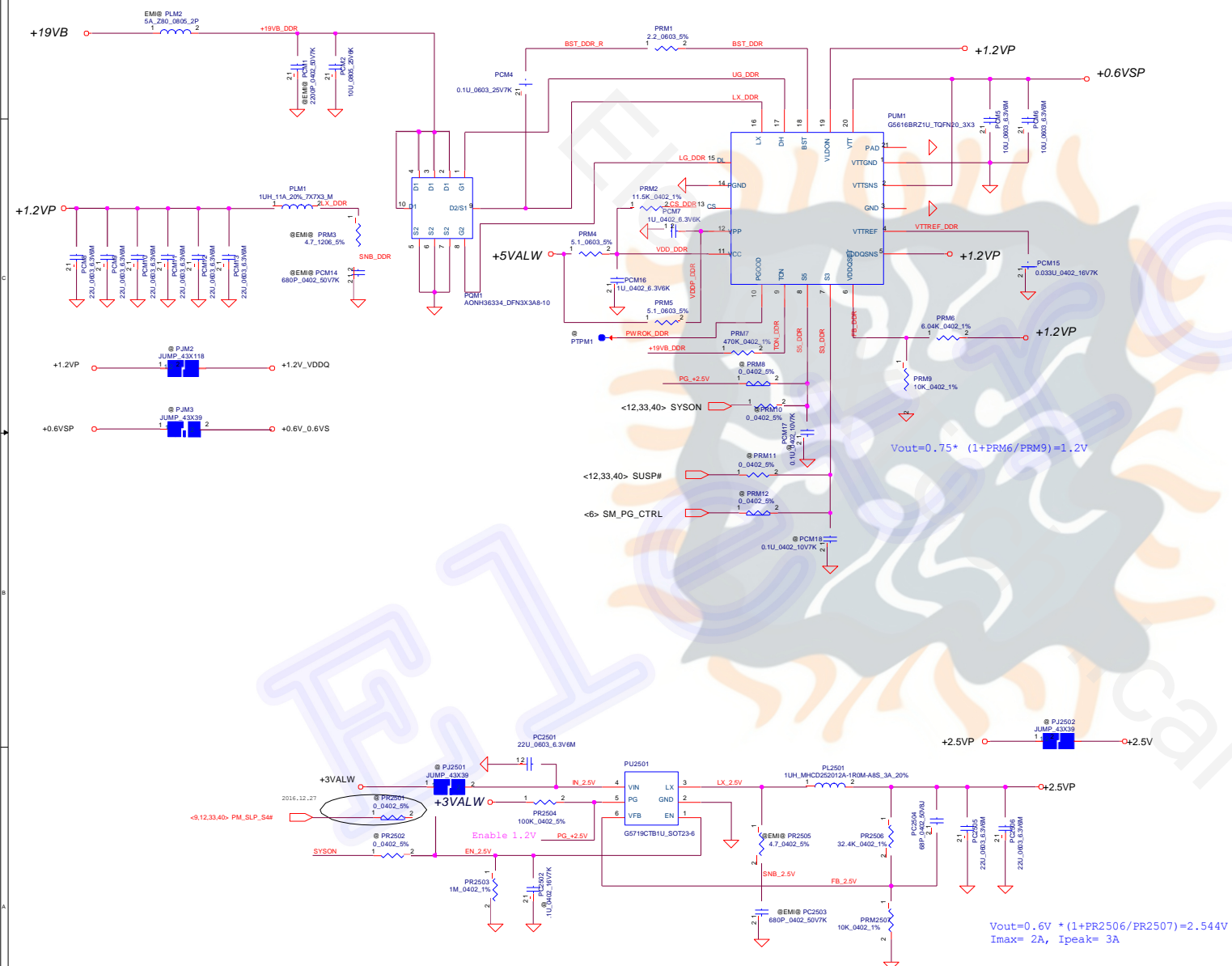


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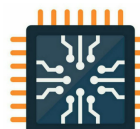


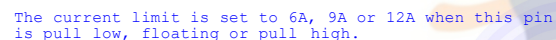
Vin Detector			
	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V
VILIM = 20*ILIM*Rsr			
ILIM = 3.3*100/(100+620)/20/0.02			
= 2.291 A			



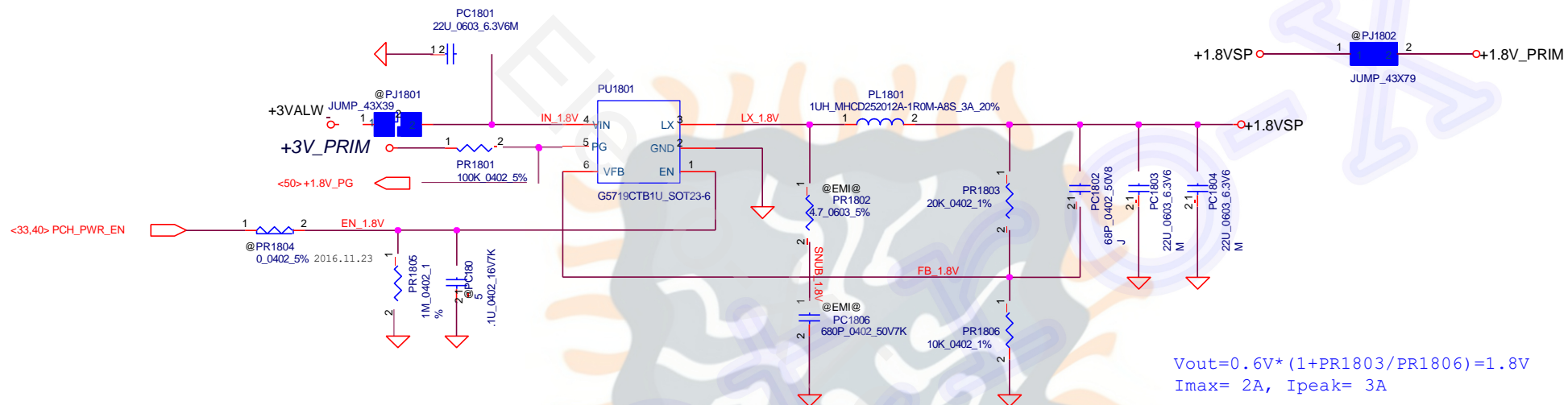


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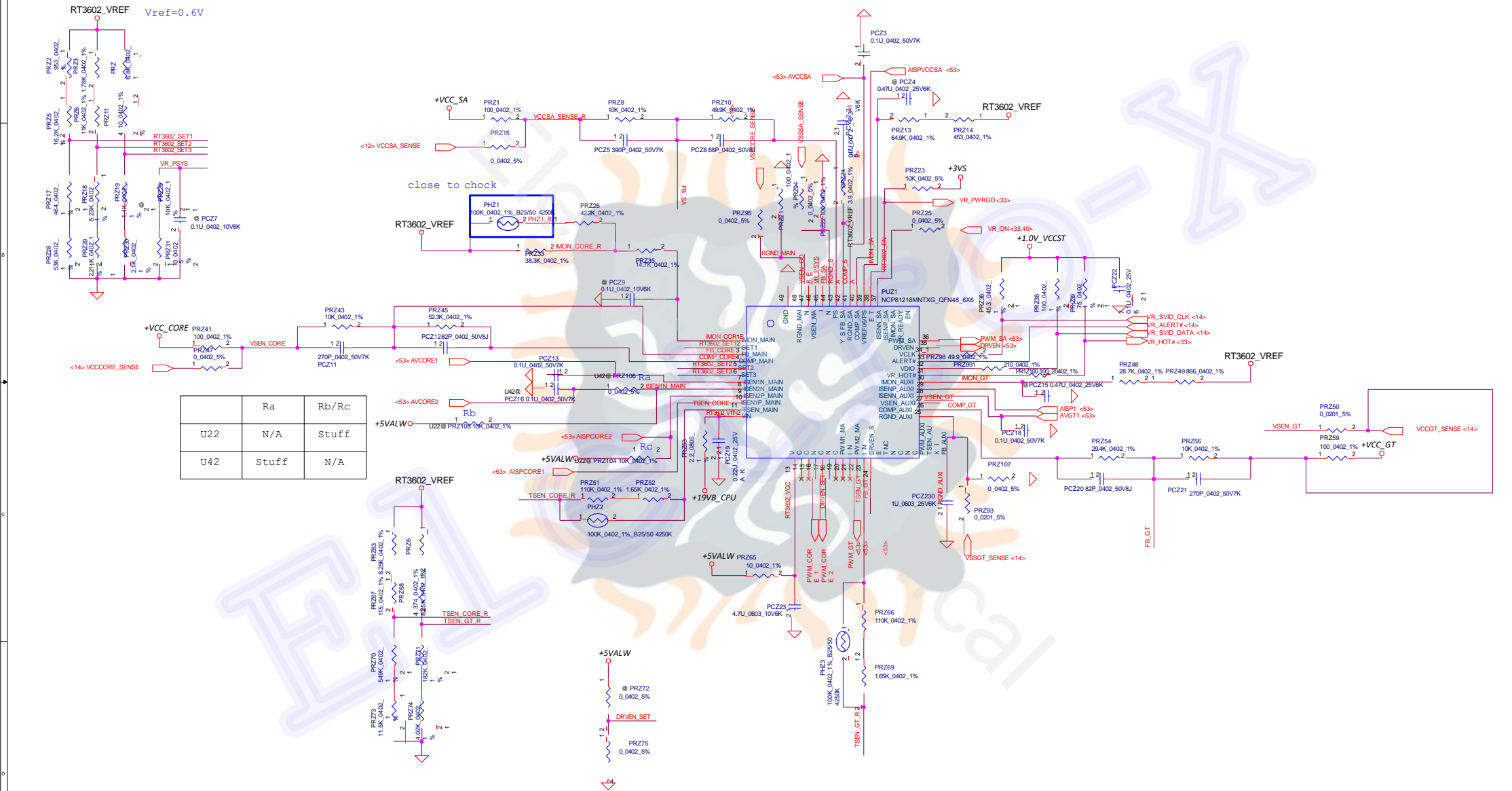


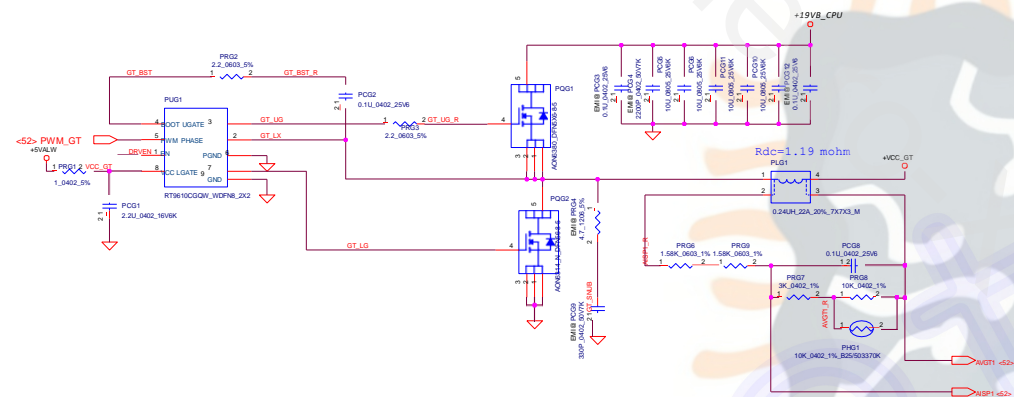
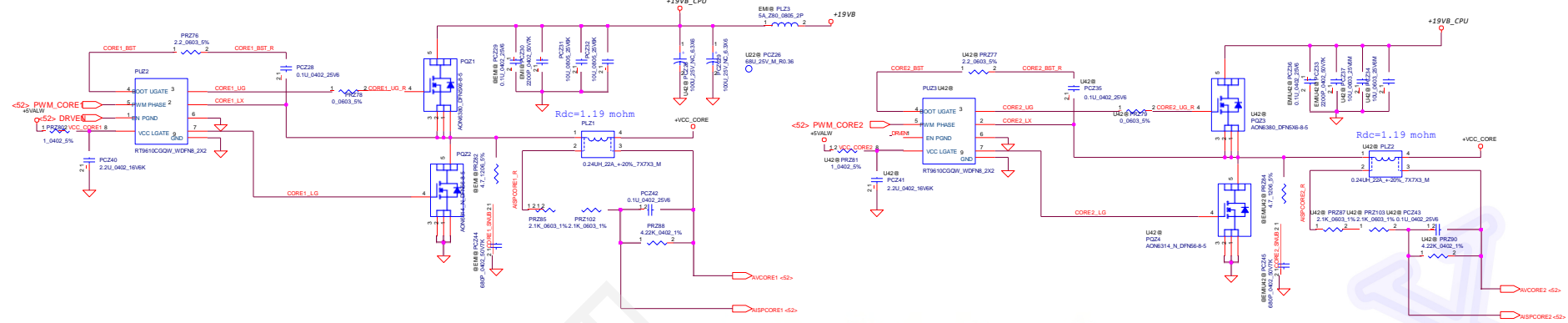


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Document Number		Rev	v0.1
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VCC CORE
FSW=500kHz
Choke=0.24uH
DCR=1.19 mohm +/- 5%

U22
LL=2.4 mohm
TDC=21A
ICCMAX=32A
OCP=40A

U42
LL=2.4 mohm
TDC=42A
ICCMAX=64A
OCP=70A

VCC GT
FSW=500kHz
Choke=0.24uH +/- 5%

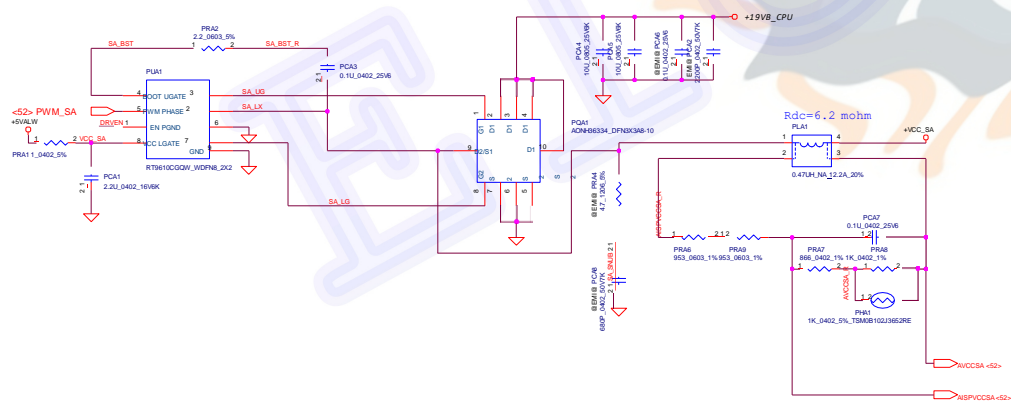
U22
LL=3.1 mohm
TDC=18A
ICCMAX=31A
OCP=39A

U42
LL=3.1 mohm
TDC=12A
ICCMAX=28A
OCP=39A

VCC SA
FSW=600kHz
DCR=6.2 mohm +/- 5%

U22
LL=10.3 mohm
TDC=4A
ICCMAX=4.5A
OCP=9.5A

U42
LL=10.3 mohm
TDC=5A
ICCMAX=5A
OCP=9.5A



+VCC_CORE

2016.12.29

VCC_CORE :
U22-
390uF*1
22uF*18
1uF*35

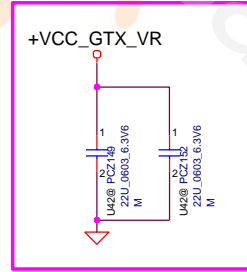
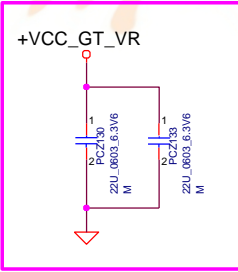
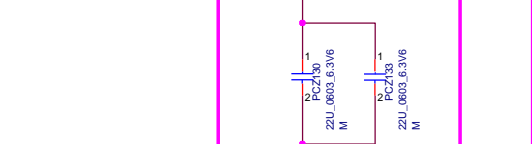
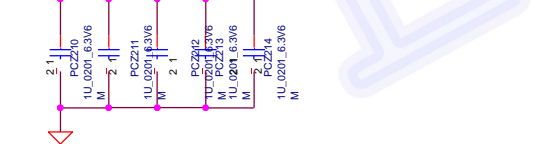
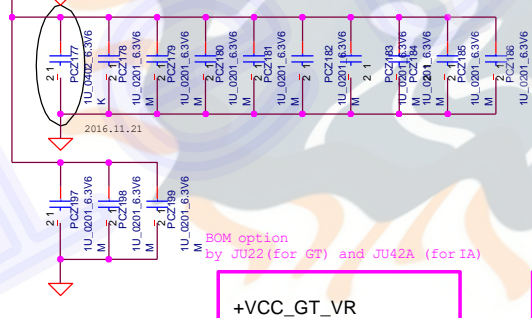
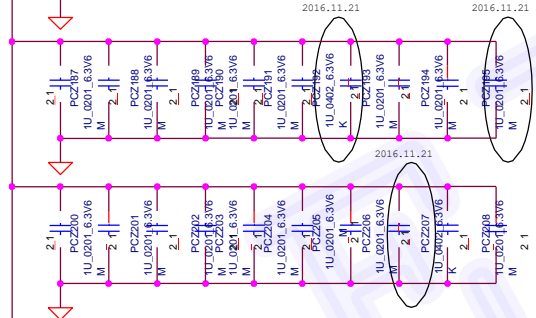
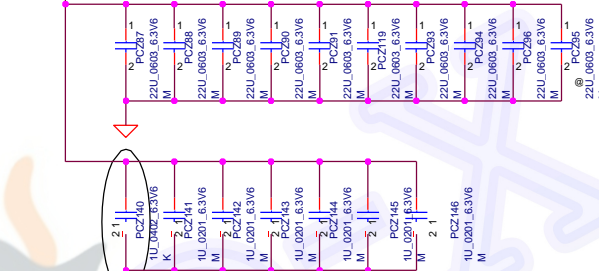
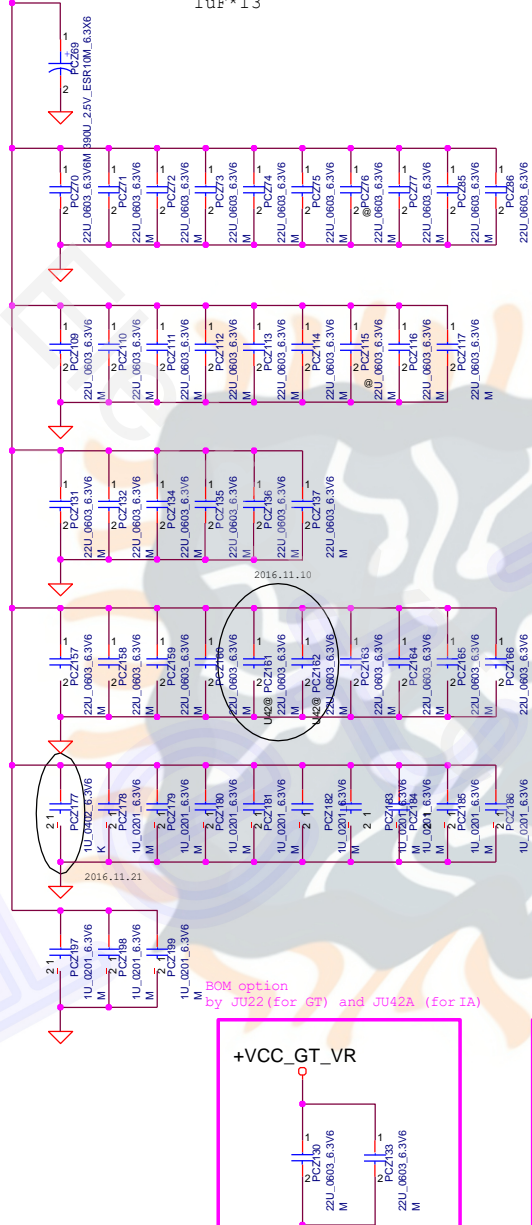
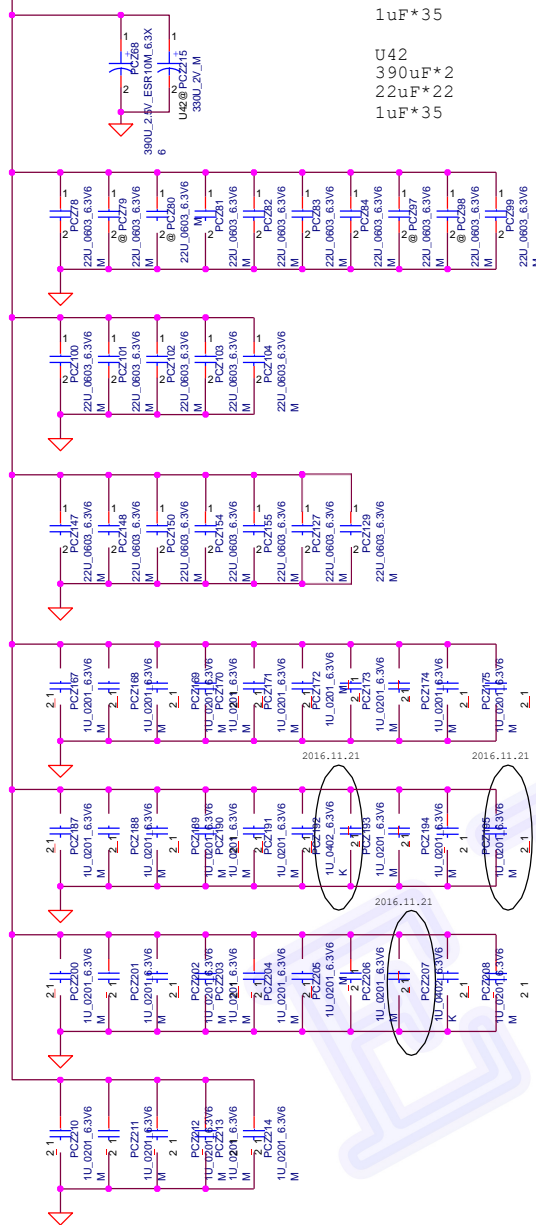
U42
390uF*2
22uF*22
1uF*35

+VCC_GT

VCC_GT :
U22- & U42
390uF*1
22uF*33
1uF*13

VCC_SA :
U22- & U42
22uF*9
1uF*7

+VCC_SA



Eletro-X Technical

Eletro-X

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